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DOT MATRIX LCD MODULE

CHARACTER TYPE — DMC SERIES

USER'S MANUAL



OPTREX CORPORATION

Preface

This user's manual concerning DMC series has been prepared for all users of OPTREX'S dot matrix LCD modules (character type DMC Series) to assist them in designing with the modules properly and efficiently.

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1. FUNCTION AND STRUCTURE

1.1 General

DMC series is the name given to the dot matrix LCD display modules that have recently been developed by OPTREX CORPORATION. The modules consist of high contrast-large viewing angle TN type LC panel, with a CMOS driver and controller, which have a low power consumption. The controller is equipped with an internal character generator ROM, RAM and RAM for display data. All display functions are controllable by instructions making the interfacing with MPU easy.

Both display data RAM and character generator RAM can be read, making it possible to use any part not used for display as general data RAM. The products of this series therefore have a wide application possibilities in the field of terminal display or display for measuring devices.

1.2 Characteristics

- (1) 5 x 7 dots + Cursor, 5 x 8 dots or 5 x 11 dots, dot matrix LCD (TN mode)
- (2) 4 bit or 8 bit interface with MPU is possible
- (3) Display data RAM 80 x 8 bit (Max 80 characters)
- (4) Character generator ROM . . . Character font 5 x 7 dots 160 kinds
Character font 5 x 10 dots 32 kinds
- (5) Character generator RAM . . . Program write (64 x 8 bit)
Character font 5 x 7 dots 8 kinds or
Character font 5 x 10 dots 4 kinds
- (6) Both display data RAM and Character generator RAM can be read from MPU
- (7) Duty ratio 1 Line Display: 1/8 duty 5x7 dots + Cursor, 5x8 dots
1/11 duty 5x11 dots
1/16 duty 5x7 dots + Cursor, 5x8 dots
2 Line Display: 1/16 duty 5x7 dots + Cursor, 5x8 dots
4 Line Display: 1/16 duty 5x8 dots
- (8) Wide variety of operating instructions:
Display clear, Cursor home, Display ON/OFF, Display character blink, Cursor shift,
Display shift.
- (9) Internal automatic reset circuit when supplied with power.
- (10) Internal oscillating circuit
- (11) CMOS process used
- (12) Logic power source: Single (+5V)
- (13) Operating temperature range: 0 ~ +50°C (Standard type)
-20 ~ +70°C ("H" type)

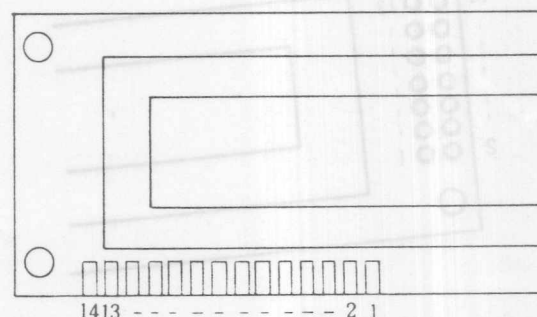
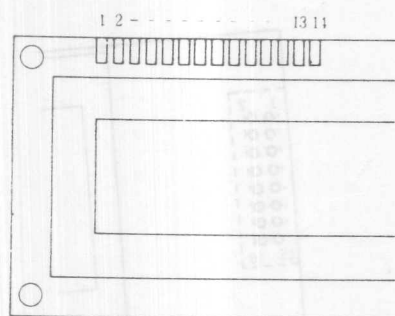
1.3 List of DMC series

Table #1

Item Model No.	Display Format	Character Font	Module Size W x H x T (mm)	View Area W x H (mm)	Character Size W x H (mm)	Dot Size W x H (mm)
DMC 16106A	16 characters x 1 line	5x11 dots	80x36x10	64.5x13	3.2x8.2	0.6x0.7
DMC 16106C	16 characters x 1 line	5x 8 dots	80x36x10	64.5x13	3.2x5.95	0.6x0.7
DMC 16117	16 characters x 1 line	5x 8 dots	80x36x10	64.5x13	3.2x5.95	0.6x0.7
DMC 16128	16 characters x 1 line	5x 7 dots + Cursor	122x33x11	99x13	4.84x9.66	0.92x1.1
DMC 16129	16 characters x 1 line	5x 7 dots + Cursor	122x33x11	99x13	4.84x9.66	0.92x1.1
DMC 16106B	16 characters x 1 line	5x 7 dots + Cursor	130x44x10	99x13	4.9x9.5	0.9x1.05
DMC 16207	16 characters x 2 lines	5x 8 dots	84x44x11	61x16	2.95x5.55	0.55x0.65
DMC 16230	16 characters x 2 lines	5x 7 dots + Cursor	122x44x11	99x24	4.84x9.66	0.92x1.1
DMC 16433	16 characters x 4 lines	5x 8 dots	87x60x11	61.8x25.2	2.95x4.75	0.55x0.55
DMC 20215	20 characters x 2 lines	5x 8 dots	116x44x11	83x18.6	3.2x5.55	0.6x0.65
DMC 20434	20 characters x 4 lines	5x 8 dots	98.0x60x11	76x25.2	2.95x4.75	0.55x0.55
DMC 24138	24 characters x 1 line	5x11 dots	118x36x11	93.5x15.8	3.2x8.2	0.6x0.7
DMC 24227	24 characters x 2 lines	5x 8 dots	118x36x11	93.5x15.8	3.2x5.55	0.6x0.65
DMC 32132	32 characters x 1 line	5x11 dots	174.5x31x11	123.5x16.5	3.2x8.2	0.6x0.7
DMC 32239	32 characters x 2 lines	5x 8 dots	174.5x31x11	141.0x16.5	3.45x5.55	0.65x0.65
DMC 32216	32 characters x 2 lines	5x 8 dots	175x44x11	130x18.6	3.2x5.55	0.6x0.65
DMC 40131	40 characters x 1 line	5x11 dots	182x33.5x11	152.5x16.5	3.2x8.2	0.6x0.7
DMC 40218	40 characters x 2 lines	5x 8 dots	182x33.5x11	152.5x16.5	3.2x5.55	0.6x0.65
DMC 40440	40 characters x 4 lines	5x 8 dots	200x70x13	165x40	3.2x5.95	0.6x0.7

1.4 Explanation of functions

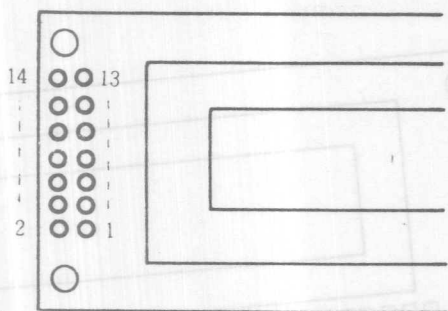
- (1) Pin positions and signal names for DMC 16106A, DMC 16106C, DMC 16117, DMC 16128, DMC 16129, DMC 16433, DMC 20434.
- (2) Pin positions and signal names for DMC 16106B, DMC 16207, DMC 16230, DMC 20215, DMC 32216.



Pin No.	Symbol
1	V _{ss}
2	V _{cc}
3	V _{ee}
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7

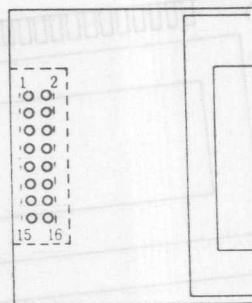
Pin No.	Symbol
1	V _{ss}
2	V _{cc}
3	V _{ee}
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7

(3) Pin positions and signal names for
DMC 24227, DMC 24138, DMC 32132,
DMC 32239, DMC 40131, DMC 40218.



Pin No.	Symbol
1	Vss
2	Vcc
3	Vee
4	RS
5	R/W
6	E
7	DB0
8	DB1
9	DB2
10	DB3
11	DB4
12	DB5
13	DB6
14	DB7

(4) Pin position and signal names for
DMC 40440.



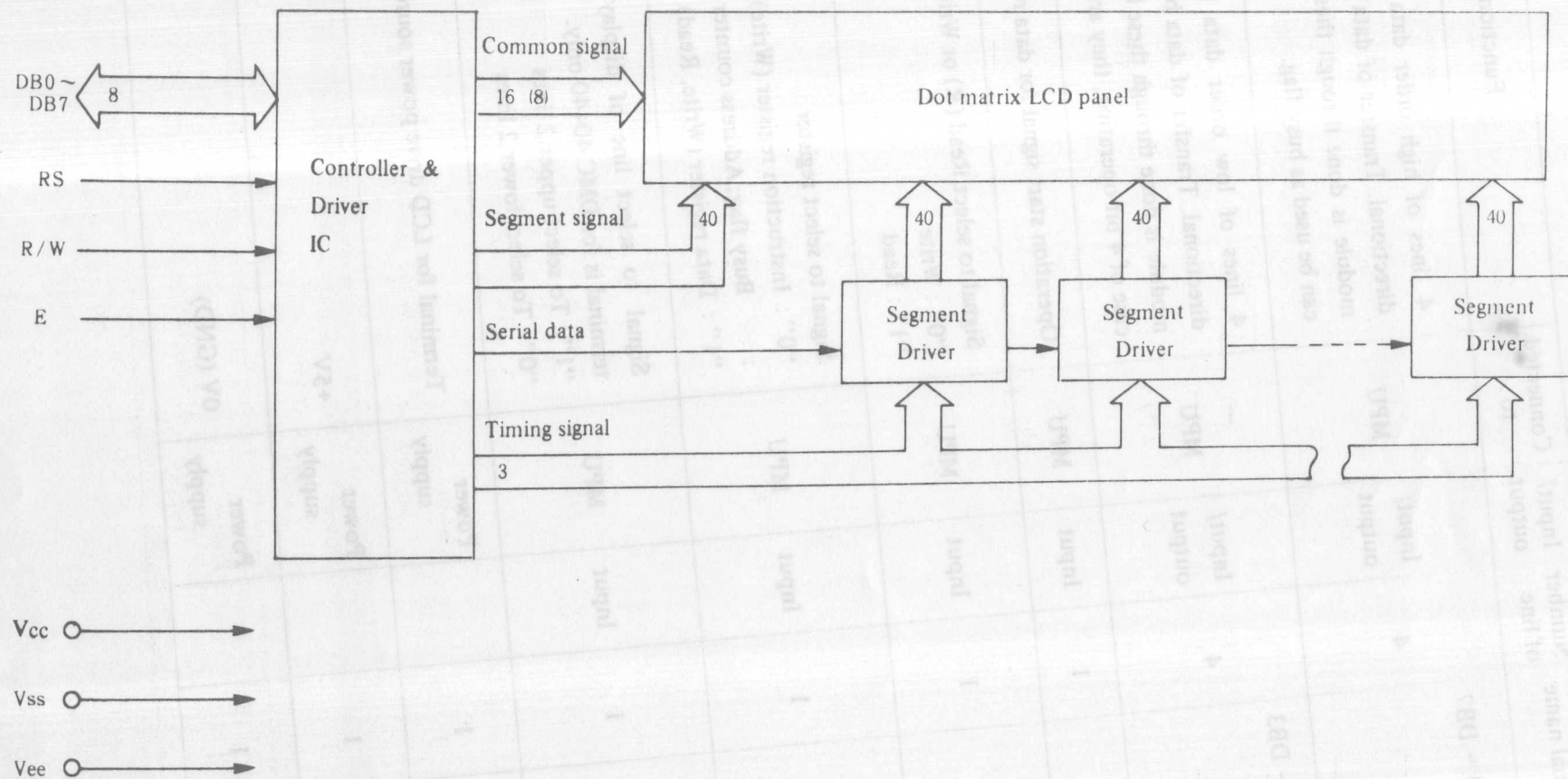
Pin No.	Symbol
1	DB7
2	DB6
3	DB5
4	DB4
5	DB3
6	DB2
7	DB1
8	DB0
9	E
10	R/W
11	RS
12	Vee
13	Vss
14	Vcc
15	LS
16	NC

Table #2 List of terminal functions

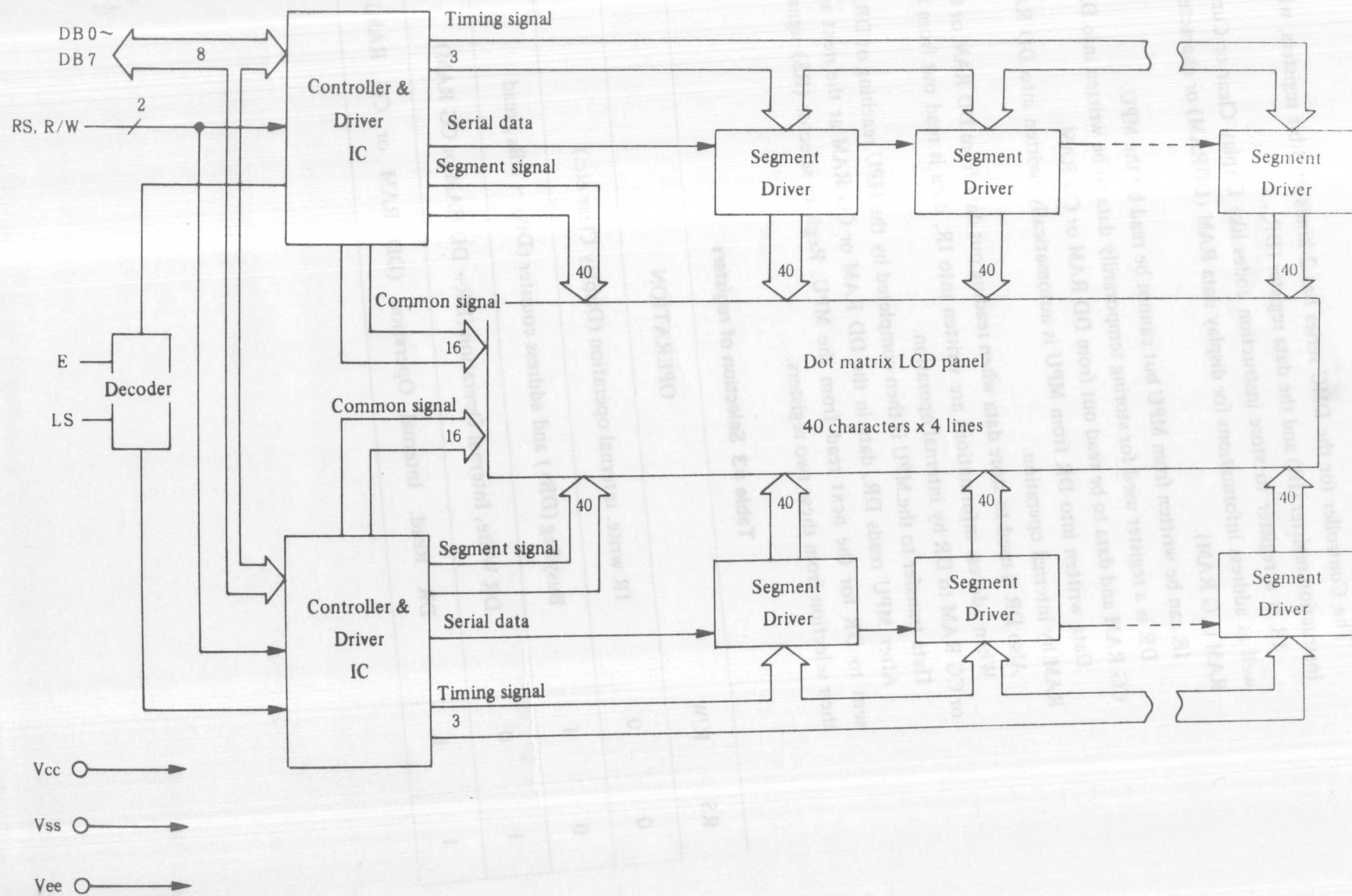
Signal name	Number of line	Input/output	Connected to	Function
DB4 ~ DB7	4	Input/output	MPU	4 lines of high order data bus. Tristate, bi-directional. Transfer of data between MPU and module is done through these lines. Also DB7 can be used as busy flag.
DB0 ~ DB3	4	Input/output	MPU	4 lines of low order data bus, Tristate, bi-directional. Transfer of data between MPU and module is done through these lines. However in case of 4 bit operation, they are not used.
E	1	Input	MPU	Operation start signal for data read/write.
R/W	1	Input	MPU	Signal to select Read (R) or Write (W) "0" : Write "1" : Read
RS	1	Input	MPU	Signal to select register "0" : Instruction register (Write) : Busy flag; Address counter (Read) "1" : Data register (Write, Read)
LS	1	Input	MPU	Signal to select line of display panel. This terminal is for DMC 40440 only. "1" : To select upper 2 lines "0" : To select lower 2 lines
Vee	1		Power supply	Terminal for LCD drive power source
Vcc	1		Power supply	+5V
Vss	1		Power supply	0V (GND)

1.5 Block diagram

(1) The modules except for DMC 40440



(2) DMC 40440.



1.6 Explanation of internal operation

(1) Register

The Controller for the DMC series has 2 kinds of 8 bit registers, which are the Instruction register (IR) and the data register (DR).

IR is a register to store instruction codes like Display Clear or Cursor Shift as well as address informations for display data RAM (DDRAM) or character generator RAM (CG RAM).

IR can be written from MPU but cannot be read by the MPU.

DR is a register used for storing temporarily data to be written into DD RAM or CG RAM and data to be read out from DD RAM or CG RAM.

Data written into DR from MPU is automatically written into DD RAM or CG RAM by internal operation.

Also DR is used to store data when reading out data from DD RAM or CG RAM.

When address informations are written into IR, data is read out from DD RAM or CG RAM to DR by internal operation.

Data transfer to the MPU is then completed by the MPU reaching of DR.

After MPU reads DR, data in the DD RAM or CG RAM at the next address is sent to DR for the next read from the MPU. Register selector (RS) signals make their selection from these two registers.

Table #3 Selection of registers

RS	R/W	OPERATION
0	0	IR write, internal operation (Display Clear etc.)
0	1	Busyflag (DB ₇) and address counter (DB ₀ ~ DB ₆) read
1	0	DR Write, Internal Operation (DR → DD RAM or CG RAM)
1	1	DR Read, Internal Operation (DD RAM or CG RAM)

(2) Busy flag (BF)

When the Busy Flag is "1", the module is in the internal operation and the next instruction will not be accepted. As shown in the Table #3, the busy flag outputs to DB₇ when RS=0, R/W=1. The next instruction must be written after ensuring that the busy flag is "0".

(3) Address Counter (AC)

The address counter (AC) assigns address to DD RAM and CG RAM.

When an instruction for address is written in IR, the address information is sent from IR to AC. The selection of either DD or CG RAM is also determined concurrently by the instruction.

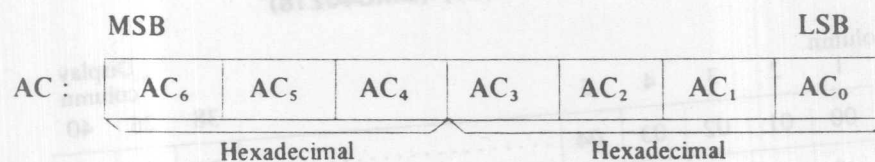
After writing into (reading from) DD RAM or CG RAM display data, address counter (AC) is automatically incremented by +1 (or decremented by -1). AC contents are outputted to DB₀ ~ DB₇ when RS=0 and R/W1 as shown in Table #3.

(4) Display data RAM (DD RAM)

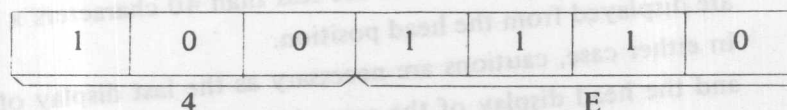
The display data RAM stores display data represented in 8-bit character code. Its capacity is 80 x 8 bits or 80 characters. The display data RAM that is not used for display can be used as a general data RAM.

Relations between DD RAM addresses and positions on the LCD are shown below.

The DD RAM address (ADD) is set in the Address Counter (AC) and is represented in hexadecimal notation.



[Example 1] DD RAM address "4E"



[Example 2] 40 columns 1 line display (DMC40131)

Column								← Display column	
	1	2	3	4	5	6		39	40
1 line	00	01	02	03	04	05		26	27
								← DD RAM Address	

(a) When the display characters are less than 80, the display begins at the head position. For example 16 columns 1 line display (1/8 duty) will be as follows:

Column										← Display column	
	1	2	3	4	5	6		14	15	16	
1 line	00	01	02	03	04	05		0D	0E	0F	← DD RAM Address

When the display shift operation is performed, the DD RAM address moves as follows:

01	02	03	04	05	06					0D	0E	0F	Left shift
4F	00	01	02	03	04					0C	0D	0E	Right shift

Other 1 line display modules more the same way.

[Example 3] 40 columns 2 lines display (DMC40218)

Column										← Display column
	1	2	3	4	5		38	26	40	
1-line	00	01	02	03	04		25	26	27	← DD RAM Address
2-line	40	41	42	43	44		65	66	67	

(a) When the display characters are less than 40 characters x 2 lines, 2 lines are displayed from the head position.

In either case, cautions are necessary as the last display of the first line and the head display of the second line are not consecution. For example, the display of 16 columns x 2 lines (1/16 duty) is as follows:

	Column						← Display column			
	1	2	3	4	5		14	15	16	
1-line	00	01	02	03	04		0D	0E	0F	← DD RAM Address
2-line	40	41	42	43	44		4D	4E	4F	

When the display shift is performed DD RAM address moves as follows

01	02	03	04	05		0E	0F	10	Left shift
41	42	43	44	45		4E	4F	50	

27	00	01	02	03		0C	0D	0E	Right shift
67	40	41	42	43		4C	4D	4E	

Other 2-line display modules move the same way.

[Example 4] 40 columns 4 lines display (DMC40440)

In case of DMC40440, the display is similar to 40 columns 2 lines and it is used by switching the upper two lines and lower two lines by LS signals. Therefore the relation between DD RAM and display columns is as follows:

Column							← Display column			
1 2 3 4 5							39	40		
Upper	1-line	00	01	02	03	04		26	27	← DD RAM Address
	2-line	40	41	42	43	44		66	67	
Lower	3-line	00	01	02	03	04		26	27	← DD RAM Address
	4-line	40	41	42	43	44		66	67	

to the
columns

Upper<Upper-

2-line us

Example 5

← Display column

(5) Character generator ROM (CG ROM)

The character generator ROM (CG ROM) is a ROM capable to generate from 8-bit character code, 5 x 7 dots or 5 x 10 dots character pattern.

The said ROM can generate 160 kinds of 5 x 7 dots or 32 kinds of 5 x 10 dots character patterns.

However cautions are requested when operating this ROM because those character fonts of 5 x 7 dots of the module will not be displayed after the 8th row of 5 x 10 dots character pattern.

Also this ROM can be modified to generate character pattern of our users choice.

For further details, please contact OPTREX sales department.

(6) Character generator RAM (CG RAM)

The character generator RAM is the RAM with which the user can rewrite character patterns by program.

With 5 x 7 dots 8 types of character patterns can be written. To display character patterns stored in CG RAM write the character codes in the left column of Table 5.1 and 5.2 in the DD RAM corresponding to the display position.

The relations between CG RAM address and data and displayed pattern are shown in Table #5.1 and 5.2 respectively.

Besides, area not used for display can be used as general data RAM'

Table #4 Correspondence between Character codes and character patterns

High order bit Low order bit	0000	0010	0011	0100	0101	0110	0111	1010	1011	1100	1101	1110	1111
0000	CG RAM		0	a	P	\	P	-	9	E	o	P	
0001	2	!	1	A	Q	a	9	7	+	4	a	9	
0010	3	"	2	B	R	b	r	T	4	9	x	P	Q
0011	4	#	3	C	S	c	s	J	5	T	E	e	o
0100	5	*	4	D	T	d	t	\	J	t	+	P	Q
0101	6	%	5	E	U	e	u	.	7	+	J	e	Q
0110	7	@	6	F	V	f	v	7	0	=	a	P	Q
0111	8	^	7	G	W	g	w	7	+	x	7	Q	Q
1000	1	(	8	H	X	h	x	4	9	+	U	7	x
1001	2	)	9	I	V	i	v	9	7	U	U	7	U
1010	3	+	;	J	Z	j	z	=	0	N	\	J	+
1011	4	+	;	K	C	k	c	4	9	E	Q	7	7
1100	5	.	<	L	+	l	l	9	9	7	Q	Q	Q
1101	6	-	=	M	J	m	j	a	z	^	Q	+	+
1110	7	.	>	N	^	n	+	a	E	+	7	7	
1111	8	/	?	O	_	o	+	u	U	7	Q	Q	

(Note) Character of high order bit 1110 and 1111 may be inadequate.

Table #5.1 Relation between CG RAM address, character codes (DD RAM) and character patterns (CG RAM data) (in case of 5 x 7 dots)

Character code (DD RAM data)	CG RAM address	Character pattern (CG RAM data)
7 6 5 4 3 2 1 0 Higher order bit Lower order bit	5 4 3 2 1 0 Higher order bit Lower order bit	7 6 5 4 3 2 1 0 Higher order bit Lower order bit
0 0 0 0 * 0 0 0	0 0 0 0 0 0 0 0 0 0 0 1 0 0 0 0 1 0 0 0 0 0 1 1 0 0 0 1 0 0 0 0 0 1 0 1 0 0 0 1 1 0 0 0 0 1 1 1	* * * 1 1 1 1 0 * * * 1 0 0 0 1 * * * 1 0 0 0 1 * * * 1 1 1 1 0 * * * 1 0 1 0 0 * * * 1 0 0 1 0 * * * 1 0 0 0 1 * * * 0 0 0 0 0 Example of character (1) Cursor position
0 0 0 0 * 0 0 1	0 0 1 0 0 0 0 0 1 0 0 1 0 0 1 0 1 0 0 0 1 0 1 1 0 0 1 1 0 0 0 0 1 1 0 1 0 0 1 1 1 0 0 0 1 1 1 1	* * * 1 0 0 0 1 * * * 0 1 0 1 0 * * * 1 1 1 1 1 * * * 0 0 1 0 0 * * * 1 1 1 1 1 * * * 0 0 1 0 0 * * * 0 0 1 0 0 * * * 0 0 0 0 0 Example of character pattern (2)
0 0 0 0 * 1 1 1	1 1 1 1 0 0 1 1 1 1 0 1 1 1 1 1 1 0 1 1 1 1 1 1	* * * * * * * * * * * *

*means
Don't care.

- Note:** (1) Character codes 0 ~ 2 Correspond to CG RAM address bit 3 ~ 5. (3 bits: 8 types)
- (2) CG RAM address bits 0 ~ 2 designate the line position of character pattern. The 8th line is the cursor position and display is performed in logical OR by the cursor. Maintain the 8th line data, corresponding to the cursor display position, in the "0" state for cursor display. When the 8th line data is "1" bit 1 lights up regardless of cursor existence.
- (3) Character pattern row positions correspond to CG RAM data bits 0 ~ 4 as shown in the figure (bit 4 being at the left end). Since CG RAM data bits 5 ~ 7 are not used for display, they can be used for the general data RAM as memory still exists.
- (4) As shown in Table 5.1 CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However as character code bit 3 is an ineffective bit the "R" display in the character pattern example is selected by character code "00" (hexadecimal) or "08" (hexadecimal).
- (5) "1" for CG RAM data corresponds to selection for display and "0" for non selection.

Table #5.2 Relation between CG RAM address, character codes (DD RAM) and character patterns (CG RAM data) (in case of 5 x 10 dots)

[illegible]

Note: (1) Character code bits 1, 2 correspond to CG RAM address bits 4, 5 (2 bits: 4 types)

(2) CG RAM address bits 0 ~ 3 designate character line position.

The 11th line is the cursor position and display is performed in logical OR with cursor.

Maintain the 11th line corresponding to the cursor display position in the "0" state for cursor display.

When the 11th line data is "1", bit 1 lights up regardless of cursor existence.

(3) Character pattern row positions are the same as 5 x 7 dot character pattern positions.

(4) As shown in Table 5.2 CG RAM character patterns are selected when character code bits 4 ~ 7 are all "0". However, since character code bit 0 and 3 are ineffective bits, the display of character pattern example is selected by character code "00" "01" "08" "09" (Hexadecimal)

(5) "1" for CG RAM data corresponds to selection for display and "0" for non-selection.

Table #6 List of instructions

Instruction	Code										Description	Execution time (max) (when fcp or fosc is 250kHz)	
	RS	R/W	DB ₇	DB ₆	DB ₅	DB ₄	DB ₃	DB ₂	DB ₁	DB ₀			
Clear Display	0	0	0	0	0	0	0	0	0	1	Clears entire display and sets DD RAM address 0 in address counter.	1.64ms	
Return Home	0	0	0	0	0	0	0	0	0	1	*	Sets DD RAM address 0 is address counter. Also returns display being shifted to original position. DD RAM contents remain unchanged.	1.64ms
Entry Mode Set	0	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display. These operations are performed during data write and read.	40μs
Display ON/OFF Control	0	0	0	0	0	0	0	1	D	C	B	Sets ON/OFF of entire display (D), cursor ON/OFF (C), and blink of cursor position character (B).	40μs
Cursor or Display Shift	0	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor and shifts display without changing DD RAM contents.	40μs
Function Set	0	0	0	0	0	1	DL	N	F	*	*	Sets interface data length (DL), number of display lines (L) and character font (F).	40μs
Set CG RAM Address	0	0	0	0	1	AGC					Sets CG RAM address. CG RAM data is sent and received after this setting.	40μs	
Set DD RAM Address	0	0	0	1	ADD					Sets DD RAM address. DD RAM data is sent and received after this setting.	40μs		
Read Busy Flag & Address	0	1	BF	AC					Reads Busy flag (BF) indicating internal operation is being performed and reads address counter contents.	40μs			
Write Data to CG or DD RAM	1	0	Write Data					Writes data into DD RAM or CG RAM.	40μs				
Read Data from CG or DD RAM	1	1	Read Data					Reads data from DD RAM or CG RAM.	40μs				
	I/D=1 : Increment I/D=0 : Decrement S=1 : Accompanies display shift. S/C=1 : Display shift S/C=0 : Cursor move R/L=1 : Shift to the right. R/L=0 : Shifts to the left. DL=1 : 8 bits, DL=0 : 4 bits. N=1 : 2 lines, N=0: 1 line F=1 : 5×10 dots, F=0: 5×7 dots BF=1 : Internally operating BF=0 : Can accept instruction										DD RAM : Display data RAM CG RAM : Character generator RAM ACC : CG RAM address ADD : DD RAM address. Corresponds to cursor address. AC : Address counter used for both DD and CG RAM address.	Execution time changes when frequency changes. (Example) When fcp or fosc is 270kHz: $40\mu s \times \frac{250}{270} = 37\mu s$	

* No Effect

1.7 Cautions when using the module

- (1) LCD panel is made of glass so please avoid subjecting to strong mechanical shock or applying strong pressure on to the surface of display area.
- (2) The polarizer used on the surface of display panel is easily scratched and damaged. Therefore please be careful when handling the module.
- (3) CMOS-LSI is used for module circuit therefore your attention is called to the following:
 - 1) All unused input terminals should be connected to Vcc or GND. The selection of Vcc or GND will depend upon which connection will satisfy the desired logical function.
 - 2) When power source voltage is not applied avoid applying input signal.
 - 3) Anti-static electricity measures
 - a. When working please be sure to either use your naked or gloved hand and wear non-conductive work suit to prevent generating static electricity by friction.
 - b. Floors, doors and work tables must be grounded to discharge electricity.
 - c. Tools such as soldering iron, cutting pliers and tweezers should be either grounded or properly treated whenever necessary.
 - (4) For long time storage, avoid places of high temperature and humidity or places under direct sunlight.
 - (5) When LCD panel is broken, do not try to taste the liquid crystal since it is poisonous.

Also, if hand and foot or suit is smeared with liquid crystal wash out the liquid crystal immediately with water.

2. INSTRUCTIONS

2.1 Detailed explanations

(1) Clear Display

	RS	R/W	DB ₇							DB ₀
Code	0	0	0	0	0	0	0	0	0	1

Writes the space code "20" (hexadecimal) into all address of DD RAM. Returns display to its original position if it was shifted. In other words the display disappears and the cursor or blink moves to the left edge of the display (the first line if 2 lines are displayed). The execution of clear display instruction sets entry mode to increment mode.

(2) Return Home

	RS	R/W	DB ₇							DB ₀
Code	0	0	0	0	0	0	0	0	1	*

*means Don't care

Sets the DD RAM address "0" in address counter. Return display to its original position if it was shifted. DD RAM contents do not change.

The cursor or the blink moves to the left edge of the display (the first line if 2 lines are displayed)

(3) Entry mode set

	RS	S/W	DB ₇							DB ₀
Code	0	0	0	0	0	0	0	1	I/D	S

I/D: Increments (I/D = 1) or decrements (I/D = 0) the DD RAM address by 1 when a character code is written into or read from the DD RAM.

The cursor or blink moves to the right when incremented by +1.

The same applies to writing and reading of CG RAM.

S: Shifts the entire display either to the right or to the left when S = 1; shift to the left when I/D = 1 and to the right when I/D = 0. Thus it looks as if the cursor stands still and only the display seems to move.

The display does not shift when reading from DD RAM nor when S = 0.

(4) Display ON/OFF Control

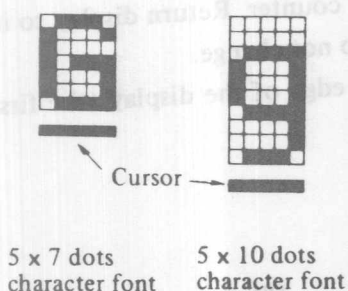
	RS	R/W	DB ₇							DB ₀
Code	0	0	0	0	0	0	1	D	C	B

D: The display is ON when D = 1 and OFF when D = 0. When OFF due to D = 0, display data remains in the DD RAM. It can be displayed immediately by setting D = 1.

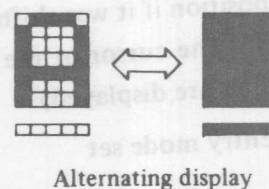
C: The cursor displays when C = 1 and does not display when C = 0.
Even if the cursor disappears, the function of I/D etc, does not change during data write.
The cursor is displayed on the 8th line when 5 × 7 dot character font has been selected.

B: The character indicated by cursor blinks when B = 1. The blink is displayed by switching between all blank dot and display characters at 0.4 sec interval.

The cursor and the blink can be set to display simultaneously.



(a) Cursor display example



(b) Blink display example

(5) Cursor or display shift

	RS	R/W	DB ₇							DB ₀
Code	0	0	0	0	0	1	S/C	R/L	*	*

*means Don't care.

(5) Cursor or display shift

Shifts cursor position or display to the right or left without writing or reading display data. This function is used to correct or search for the display. In a 2-line display the cursor moves to the 2nd line when it passes the 40th digit of the 1st line. Notice that the 1st and 2nd line displays will shift at the same time.

When the displayed data is shifted repeatedly each line only moves horizontally but the 2nd line display does not shift into the 1st line position.

S/C	R/L	
0	0	Shifts cursor position to the left (AC is decremented by one)
0	1	Shifts cursor position to the right (AC is incremented by one)
1	0	Shifts the entire display to the left. The cursor follows the display shift.
1	1	Shifts the entire display to the right. The cursor follows the display shift.

The contents of Address Counter (AC) do not change if the only action performed is shifting display.

(6) Function set

(a) 1-line display

	RS	R/W	DB ₇						DB ₀	
Code	0	0	0	0	1	DL	0	F	*	*

* means Don't care

(b) 2-line display

	RS	R/W	DB ₇						DB ₀	
Code	0	0	0	0	1	DL	1	*	*	*

* means Don't-care

DL: Sets interface data length. Data are sent or received in 8 bits length ($DB_7 \sim DB_0$) when $DL = '1'$ and in 4 bits length ($DB_7 \sim DB_4$) when $DL = 0$.

When the 4 bits length is selected, data must be sent or received twice.

F: Sets character font.

F = "1" : 5 x 10 dots

F = "0" : 5 x 7 dots

Note: 1) Perform the function at the head of the program before executing all instructions (except "Busy flag/address read"). From this point, the function set instruction cannot be executed other than to change interface length.

2) When power supply is applied the following initial setting is automatically set regardless of types of modules.

(i) Display clear

(ii) Function set

Interface data length 8 bits

1-line display

(iii) Display ON/OFF Control

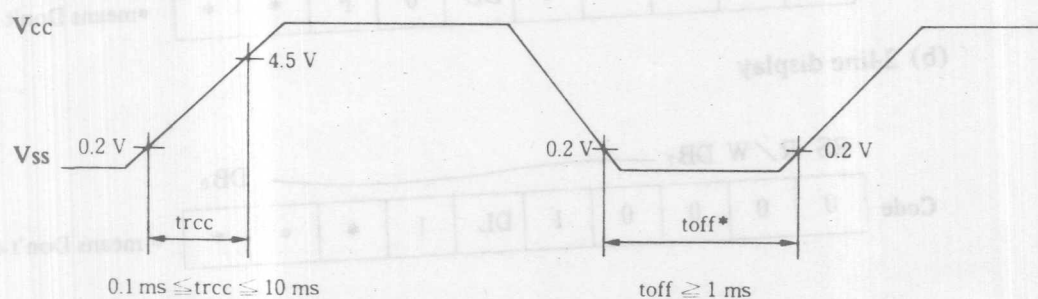
Display OFF, Cursor OFF, Blink OFF.

(iv) Entry mode set

No increment or shift.

Therefore in case of 2 (4) lines display module, it is necessary to execute function set again.

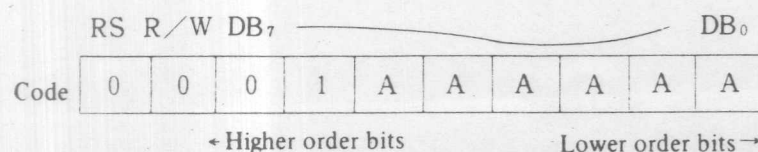
3) To correctly operate the initial setting the following conditions for the power source are necessary.



* Toff stipulates the time of power OFF for power supply instantaneous cut off or when the power supply repeats ON/OFF.

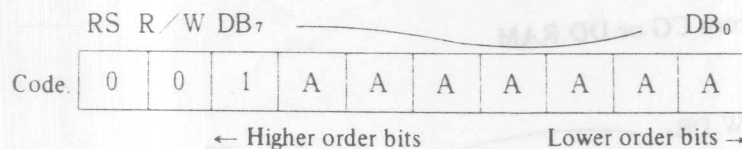
If the above conditions are not satisfied automatic initial setting cannot be performed. In that case execute initial setting with instructions.

(7) Set CG RAM address



Sets CG RAM address into the address counter in binary AAAAAAA and then data is written or read from the MPU for the CG RAM.

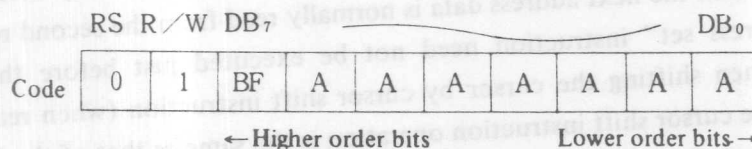
(8) Set DD RAM address



Sets the DD RAM address into the address counter in binary AAAAAAA Data is then written or read from the MPU for the DD RAM.

However, for 1-line display module AAAAAAA is "00" ~ "4F" (hexadecimal) for 2-line display module AAAAAAA is "00" ~ "27" (hexadecimal) for the first line and "40" ~ "67" (hexadecimal) for the second line.

(9) Read busy flag and address

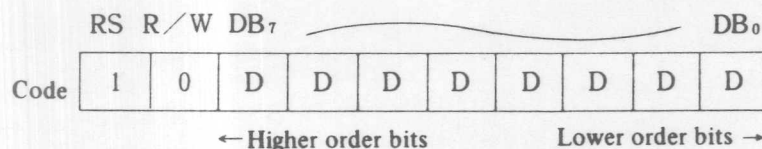


Reads the busy flag (BF) that indicates the system is none internally operating by a previously received instruction. BF = 1 indicates that internal operation is in progress and the next instruction will not be accepted until BF is set to "0".

Check the BF status before the next write operation.

At the same time the value of the address counter expressed in binary AAAAAAA is read out. The address counter is used by both CG and DD RAM and its value is determined by the previous instruction. Address contents are the same as in items (7) and (8).

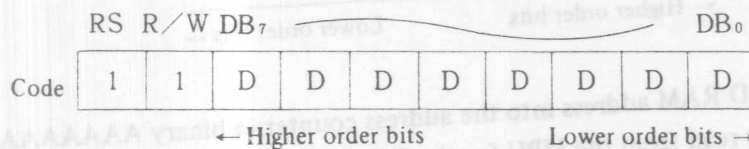
(10) Write data to CG or DD RAM



Writes binary 8 bits data DDDDDDDD to the CG or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read (CG RAM address set or DD RAM address set). After a write the entry mode will automatically increases or decreases the address by 1. Display shift also follows the entry mode.

(11) Read data from CG or DD RAM



Reads binary 8 bits data DDDDDDDD from the CG RAM or DD RAM.

The previous designation determines whether the CG or DD RAM is to be read.

Before entering the read instruction, you must execute either the CG RAM or DD RAM address set instruction.

If you don't, the first read data will be invalidated. When serially executing the "read" instruction the next address data is normally read from the second read.

The "address set" instruction need not be executed just before the "read" instruction when shifting the cursor by cursor shift instruction (when reading out DD RAM). The cursor shift instruction operation is the same as that of the DD RAM address set instruction.

After a read, the entry mode automatically increases or decreases the address by 1. However display shift is not executed no matter what the entry mode is.

Note: The address counter (AC) is automatically incremented or decremented by 1 after "write" instructions to either CG RAM or DD RAM. RAM data selected by the AC cannot then be read out even if "read" instructions are executed.

The conditions for correct data read out are: execute either the address set instruction or cursor shift instruction (only with DD RAM) or the execution of the "read" instruction from the second time when the read instruction is serial.

2.2 Examples of instructions

(1) Using DMC 16106C DMC 16129, DMC 16106B (1-line display)

No.	Instruction	Display	Operation										
1	Power supply ON (Initialized by Internal reset circuit)	<table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀						Module is initialized. No display appears.
RS	R/W	DB ₇	~	DB ₀									
2	Function set	<table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td></td><td></td><td>0 0 1 1 0 0</td><td>*</td><td>*</td></tr></table>	RS	R/W	DB ₇	~	DB ₀			0 0 1 1 0 0	*	*	Sets interface data length and selects 5 x 7 dots 1-line display
RS	R/W	DB ₇	~	DB ₀									
		0 0 1 1 0 0	*	*									
3	Display ON/OFF Control	<table><tr><td>R S</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0 0 0 0</td><td>1 1 1</td><td>0</td></tr></table>	R S	R/W	DB ₇	~	DB ₀	0	0	0 0 0 0	1 1 1	0	Turns on display and cursor. No display appears
R S	R/W	DB ₇	~	DB ₀									
0	0	0 0 0 0	1 1 1	0									
4	Entry mode set	<table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0 0 0 0</td><td>0 1 1</td><td>0</td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	0 0 0 0	0 1 1	0	Sets mode to increment the address by one and to shift cursor to the right at the time of write to internal RAM.
RS	R/W	DB ₇	~	DB ₀									
0	0	0 0 0 0	0 1 1	0									
5	Write data to CG/DD RAM	<table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0 1 0 0</td><td>1 1 0 0</td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀	1	0	0 1 0 0	1 1 0 0		Writes "L" cursor is incre- mented and moves to the right.
RS	R/W	DB ₇	~	DB ₀									
1	0	0 1 0 0	1 1 0 0										
6	Write data to CG/DD RAM	<table><tr><td>R/S</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0 1 0 0</td><td>0 0 1 1</td><td></td></tr></table>	R/S	R/W	DB ₇	~	DB ₀	1	0	0 1 0 0	0 0 1 1		Writes "C"
R/S	R/W	DB ₇	~	DB ₀									
1	0	0 1 0 0	0 0 1 1										
7													
8	Write to data to CG/DD RAM	<table><tr><td>R S</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0 0 1 1</td><td>0 1 1 0</td><td></td></tr></table>	R S	R/W	DB ₇	~	DB ₀	1	0	0 0 1 1	0 1 1 0		Writes "6" cursor disappears. (DD RAM address is 10H)
R S	R/W	DB ₇	~	DB ₀									
1	0	0 0 1 1	0 1 1 0										

No.	Instruction	Display	Operation										
9	DD RAM address set <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>1 0 0 0 0 0 0 0</td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	1 0 0 0 0 0 0 0			LCD MODULE DMC1	Cursor appears at home position
RS	R/W	DB ₇	~	DB ₀									
0	0	1 0 0 0 0 0 0 0											
10	Cursor/Display shift <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0 0 0 1 1 1 * *</td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	0 0 0 1 1 1 * *			LCD MODULE DMC	Entire display shifts to the right by one digit.
RS	R/W	DB ₇	~	DB ₀									
0	0	0 0 0 1 1 1 * *											
11	Cursor/Display shift <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0 0 0 1 1 1 * *</td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	0 0 0 1 1 1 * *			LCD MODULE DMC	Entire display shifts one digit to the right.
RS	R/W	DB ₇	~	DB ₀									
0	0	0 0 0 1 1 1 * *											
12	Display ON/OFF cursor <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0 0 0 0 1 0 0 0</td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	0 0 0 0 1 0 0 0				Entire display disappears.
RS	R/W	DB ₇	~	DB ₀									
0	0	0 0 0 0 1 0 0 0											
13	Display ON/OFF <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0 0 0 0 1 1 1 0</td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	0 0 0 0 1 1 1 0			LCD MODULE DMC16	Entire display reappears.
RS	R/W	DB ₇	~	DB ₀									
0	0	0 0 0 0 1 1 1 0											
14	Cursor Home <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0 0 0 0 0 0 1 *</td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	0 0 0 0 0 0 1 *			LCD MODULE DMC16	Returns both cursor and display to original position.
RS	R/W	DB ₇	~	DB ₀									
0	0	0 0 0 0 0 0 1 *											
15	Display clear <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0 0 0 0 0 0 0 1</td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	0 0 0 0 0 0 0 1			-	Clears entire display except cursor.
RS	R/W	DB ₇	~	DB ₀									
0	0	0 0 0 0 0 0 0 1											
16													

(2) When employing DMC16207, DMC16230 (2-line display)

No.	Instruction	Display	Operation												
1	Power supply ON (Initialized by internal circuit) <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀						<table><tr><td></td></tr><tr><td></td></tr></table>			Module is initialized.
RS	R/W	DB ₇	~	DB ₀											
2	Function Set <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0 0 1 1 1</td><td>*</td><td>*</td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	0 0 1 1 1	*	*	<table><tr><td></td></tr><tr><td></td></tr></table>			Sets the interface data length to 8 bits and selects 2-line display and 5 × 7-dot character font.
RS	R/W	DB ₇	~	DB ₀											
0	0	0 0 1 1 1	*	*											
3	Display ON/OFF control <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0 0 0 0 1 1 1</td><td>0</td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	0 0 0 0 1 1 1	0		<table><tr><td>—</td></tr><tr><td></td></tr></table>	—		Turns on display and cursor. No display appears.
RS	R/W	DB ₇	~	DB ₀											
0	0	0 0 0 0 1 1 1	0												
—															
4	Entry mode set <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0 0 0 0 0 1 1 1</td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	0 0 0 0 0 1 1 1			<table><tr><td>—</td></tr><tr><td></td></tr></table>	—		Sets mode to increment address by one and to shift the cursor to the right at the time of write to internal RAM
RS	R/W	DB ₇	~	DB ₀											
0	0	0 0 0 0 0 1 1 1													
—															
5	Write data to CG/DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0 1 0 0 1 1 0 0</td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀	1	0	0 1 0 0 1 1 0 0			<table><tr><td>L _</td></tr><tr><td></td></tr></table>	L _		Writes "L". Cursor is incremented by one and shifts to the right.
RS	R/W	DB ₇	~	DB ₀											
1	0	0 1 0 0 1 1 0 0													
L _															
6	Write data to CG/DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0 1 0 0 0 0 1 1</td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀	1	0	0 1 0 0 0 0 1 1			<table><tr><td>LC _</td></tr><tr><td></td></tr></table>	LC _		Writes "C"
RS	R/W	DB ₇	~	DB ₀											
1	0	0 1 0 0 0 0 1 1													
LC _															
7															
8	Write data to CG/DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0 0 1 1 0 1 1 0</td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₀	1	0	0 0 1 1 0 1 1 0			<table><tr><td>LCD MODULE DMC16</td></tr><tr><td></td></tr></table>	LCD MODULE DMC16		Writes "6"
RS	R/W	DB ₇	~	DB ₀											
1	0	0 0 1 1 0 1 1 0													
LCD MODULE DMC16															

No.	Instruction	Display	Operation										
9	Set DD RAM address <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0 0 0 0 0 0 0</td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	1	1	0 0 0 0 0 0 0	LCD MODULE DMC16 —	Sets RAM address so that the cursor is positioned at the head of the 2nd line.
RS	R/W	DB ₇	~	DB ₀									
0	0	1	1	0 0 0 0 0 0 0									
10	Write data to CG/DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1 1 0 0 1 1</td></tr></table>	RS	R/W	DB ₇	~	DB ₀	1	0	0	0	1 1 0 0 1 1	LCD MODULE DMC16 3_	White "3"
RS	R/W	DB ₇	~	DB ₀									
1	0	0	0	1 1 0 0 1 1									
11	Write data to CG/DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1 1 0 0 1 0</td></tr></table>	RS	R/W	DB ₇	~	DB ₀	1	0	0	0	1 1 0 0 1 0	LCD MODULE DMC16 32_	Writes "2"
RS	R/W	DB ₇	~	DB ₀									
1	0	0	0	1 1 0 0 1 0									
12													
13	Write data to CG/DD RAM address <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>1 0 1 0 1 0</td></tr></table>	RS	R/W	DB ₇	~	DB ₀	1	0	0	0	1 0 1 0 1 0	LCD MODULE DMC16 32 DIGITS, 2 LINES _	Writes "S"
RS	R/W	DB ₇	~	DB ₀									
1	0	0	0	1 0 1 0 1 0									
14	Set DD/RAM address <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>1</td><td>0</td><td>0 0 0 0 0 0 0</td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	1	0	0 0 0 0 0 0 0	LCD MODULE DMC16 32 DIGITS, 2 LINES	Moves cursor to original position
RS	R/W	DB ₇	~	DB ₀									
0	0	1	0	0 0 0 0 0 0 0									
15	Clear display <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0 0 0 0 0 0 1</td></tr></table>	RS	R/W	DB ₇	~	DB ₀	0	0	0	0	0 0 0 0 0 0 1	—	Return both display and cursor to the original position
RS	R/W	DB ₇	~	DB ₀									
0	0	0	0	0 0 0 0 0 0 1									
16													

(3) When DMC 40440 is employed (4-line display)

No.	Instruction	Display	Operation												
1	Power supply ON (Initialization) <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td></td><td></td><td></td></tr></table> <table><tr><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td></td><td></td><td></td></tr></table>	LS	RS	R/W				DB ₇	~	DB ₀					Initialized by internal reset circuit.
LS	RS	R/W													
DB ₇	~	DB ₀													
2	Function set <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>1</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0 1 1 1</td><td>* * *</td></tr></table>	LS	RS	R/W	1	0	0	DB ₇	~	DB ₀	0	0 1 1 1	* * *		Sets the controller of the higher order 2-line to 8-bit interface data length and 5x7 dots character font.
LS	RS	R/W													
1	0	0													
DB ₇	~	DB ₀													
0	0 1 1 1	* * *													
3	Function set <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0 1 1 1</td><td>* * *</td></tr></table>	LS	RS	R/W	0	0	0	DB ₇	~	DB ₀	0	0 1 1 1	* * *		Sets the controller of the lower order 2-line to 8-bit interface data length and 5x7 dots character font.
LS	RS	R/W													
0	0	0													
DB ₇	~	DB ₀													
0	0 1 1 1	* * *													
4	Display ON/OFF control <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>1</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0 0 0 0 1 1 1</td><td>0</td></tr></table>	LS	RS	R/W	1	0	0	DB ₇	~	DB ₀	0	0 0 0 0 1 1 1	0		Turns on the display of higher order 1-line and the cursor. No display appears.
LS	RS	R/W													
1	0	0													
DB ₇	~	DB ₀													
0	0 0 0 0 1 1 1	0													
5	Display ON/OFF control <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td></td><td></td><td></td></tr></table>	LS	RS	R/W	0	0	0	DB ₇	~	DB ₀					Turns on the display of the lower order 2-line and turns off the cursor.
LS	RS	R/W													
0	0	0													
DB ₇	~	DB ₀													
6	Entry mode set <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>1</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td>~</td><td>DB₀</td></tr><tr><td>0</td><td>0 0 0 0 0 1 1</td><td>0</td></tr></table>	LS	RS	R/W	1	0	0	DB ₇	~	DB ₀	0	0 0 0 0 0 1 1	0		For the higher order 2-line, address is incremented by one at the time of write to internal RAM and cursor shifts to the right. Display is not shifted.
LS	RS	R/W													
1	0	0													
DB ₇	~	DB ₀													
0	0 0 0 0 0 1 1	0													

No.	Instruction	Display	Operation																									
7	Entry mode set <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td colspan="5">~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr></table>	LS	RS	R/W	0	0	0	DB ₇	~					DB ₀	0	0	0	0	0	1	1	0	<table><tr><td>—</td></tr><tr><td> </td></tr><tr><td> </td></tr><tr><td> </td></tr></table>	—				For the lower order 2-line, address is incremented by one and shifts the cursor to the right at the time of write to internal RAM.
LS	RS	R/W																										
0	0	0																										
DB ₇	~					DB ₀																						
0	0	0	0	0	1	1	0																					
—																												
8	Write to CG/DD RAM <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td colspan="5">~</td><td>DB₀</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr></table>	LS	RS	R/W	1	1	0	DB ₇	~					DB ₀	0	1	0	0	1	1	0	0	<table><tr><td>L—</td></tr><tr><td> </td></tr><tr><td> </td></tr><tr><td> </td></tr></table>	L—				Writes "L" Cursor is incremented by one and is shifted to the right.
LS	RS	R/W																										
1	1	0																										
DB ₇	~					DB ₀																						
0	1	0	0	1	1	0	0																					
L—																												
9																												
10	<table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td colspan="5">~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	LS	RS	R/W	1	1	0	DB ₇	~					DB ₀	0	0	1	1	0	0	0	0	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td> </td></tr><tr><td> </td></tr><tr><td> </td></tr></table>	LCD MODULE DMC40				Writes "0"
LS	RS	R/W																										
1	1	0																										
DB ₇	~					DB ₀																						
0	0	1	1	0	0	0	0																					
LCD MODULE DMC40																												
11	Set DD RAM address <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>1</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td colspan="5">~</td><td>DB₀</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	LS	RS	R/W	1	0	0	DB ₇	~					DB ₀	1	1	0	0	0	0	0	0	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td> </td></tr><tr><td> </td></tr><tr><td> </td></tr></table>	LCD MODULE DMC40				Sets address so that cursor comes to the 1st digit of the 2nd line.
LS	RS	R/W																										
1	0	0																										
DB ₇	~					DB ₀																						
1	1	0	0	0	0	0	0																					
LCD MODULE DMC40																												
12	Write data to CG/DD RAM <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td colspan="5">~</td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td></tr></table>	LS	RS	R/W	1	1	0	DB ₇	~					DB ₀	0	0	1	1	0	0	0	1	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>1—</td></tr><tr><td> </td></tr><tr><td> </td></tr></table>	LCD MODULE DMC40	1—			Writes "1"
LS	RS	R/W																										
1	1	0																										
DB ₇	~					DB ₀																						
0	0	1	1	0	0	0	1																					
LCD MODULE DMC40																												
1—																												

No.	Instruction	Display	Operation																							
13																										
14	Write data to CG/DD RAM <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>1</td><td>1</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td></td><td>~</td><td></td><td>DB₀</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>1</td></tr></table>	LS	RS	R/W	1	1	0	DB ₇		~		DB ₀	0	1	0	1	0	0	1	1	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES –</td></tr><tr><td></td></tr><tr><td></td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES –			Writes “S”
LS	RS	R/W																								
1	1	0																								
DB ₇		~		DB ₀																						
0	1	0	1	0	0	1	1																			
LCD MODULE DMC40																										
160 DIGITS, 4 LINES –																										
15	Display ON/OFF control <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>1</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td></td><td>~</td><td></td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr></table>	LS	RS	R/W	1	0	0	DB ₇		~		DB ₀	0	0	0	0	1	1	0	0	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES</td></tr><tr><td></td></tr><tr><td></td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES			The higher order 2-line is OFF
LS	RS	R/W																								
1	0	0																								
DB ₇		~		DB ₀																						
0	0	0	0	1	1	0	0																			
LCD MODULE DMC40																										
160 DIGITS, 4 LINES																										
16	Set DD RAM address <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td></td><td>~</td><td></td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	LS	RS	R/W	0	0	0	DB ₇		~		DB ₀	1	0	0	0	0	0	0	0	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES</td></tr><tr><td></td></tr><tr><td></td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES			DD RAM address is set at the 1st digit of the 3rd line.
LS	RS	R/W																								
0	0	0																								
DB ₇		~		DB ₀																						
1	0	0	0	0	0	0	0																			
LCD MODULE DMC40																										
160 DIGITS, 4 LINES																										
17	Diaplay ON/OFF control <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td></td><td>~</td><td></td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr></table>	LS	RS	R/W	0	0	0	DB ₇		~		DB ₀	0	0	0	0	1	1	1	0	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES</td></tr><tr><td>–</td></tr><tr><td></td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES	–		The cursor is ON at the 1st digit of the 3rd line.
LS	RS	R/W																								
0	0	0																								
DB ₇		~		DB ₀																						
0	0	0	0	1	1	1	0																			
LCD MODULE DMC40																										
160 DIGITS, 4 LINES																										
–																										
18	Write data to CG/DD RAM address <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>0</td><td>1</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td></td><td>~</td><td></td><td>DB₀</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr></table>	LS	RS	R/W	0	1	0	DB ₇		~		DB ₀	0	1	0	0	1	0	0	0	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES</td></tr><tr><td>H_</td></tr><tr><td></td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES	H_		“Writes “H”
LS	RS	R/W																								
0	1	0																								
DB ₇		~		DB ₀																						
0	1	0	0	1	0	0	0																			
LCD MODULE DMC40																										
160 DIGITS, 4 LINES																										
H_																										

No.	Instruction	Display	Operation																										
19	Write data to CG/DD RAM <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>0</td><td>1</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td colspan="4">~</td><td colspan="3">DB₀</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr></table>	LS	RS	R/W	0	1	0	DB ₇	~				DB ₀			0	1	0	0	1	0	0	1	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES</td></tr><tr><td>HI_</td></tr><tr><td> </td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES	HI_		Writes "I".
LS	RS	R/W																											
0	1	0																											
DB ₇	~				DB ₀																								
0	1	0	0	1	0	0	1																						
LCD MODULE DMC40																													
160 DIGITS, 4 LINES																													
HI_																													
20																													
21	Write data to CG/DD RAM <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>0</td><td>1</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td colspan="4">~</td><td colspan="3">DB₀</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr></table>	LS	RS	R/W	0	1	0	DB ₇	~				DB ₀			0	1	0	1	0	1	0	0	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES</td></tr><tr><td>HIGH CONTRAST -</td></tr><tr><td> </td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES	HIGH CONTRAST -		Writes "T".
LS	RS	R/W																											
0	1	0																											
DB ₇	~				DB ₀																								
0	1	0	1	0	1	0	0																						
LCD MODULE DMC40																													
160 DIGITS, 4 LINES																													
HIGH CONTRAST -																													
22	Set DD RAM address <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td colspan="4">~</td><td colspan="3">DB₀</td></tr><tr><td>1</td><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	LS	RS	R/W	0	0	0	DB ₇	~				DB ₀			1	1	0	0	0	0	0	0	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES</td></tr><tr><td>HIGH CONTRAST</td></tr><tr><td>-</td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES	HIGH CONTRAST	-	The cursor moves to the 1st digit of the 4th line.
LS	RS	R/W																											
0	0	0																											
DB ₇	~				DB ₀																								
1	1	0	0	0	0	0	0																						
LCD MODULE DMC40																													
160 DIGITS, 4 LINES																													
HIGH CONTRAST																													
-																													
23	Write data to CG/DD RAM <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>0</td><td>1</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td colspan="4">~</td><td colspan="3">DB₀</td></tr><tr><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>1</td><td>1</td><td>1</td></tr></table>	LS	RS	R/W	0	1	0	DB ₇	~				DB ₀			0	1	0	1	0	1	1	1	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES</td></tr><tr><td>HIGH CONTRAST</td></tr><tr><td>W_</td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES	HIGH CONTRAST	W_	Writes "W".
LS	RS	R/W																											
0	1	0																											
DB ₇	~				DB ₀																								
0	1	0	1	0	1	1	1																						
LCD MODULE DMC40																													
160 DIGITS, 4 LINES																													
HIGH CONTRAST																													
W_																													
24	<table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>0</td><td>1</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td colspan="4">~</td><td colspan="3">DB₀</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>1</td></tr></table>	LS	RS	R/W	0	1	0	DB ₇	~				DB ₀			0	1	0	0	1	0	0	1	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES</td></tr><tr><td>HIGH CONTRAST</td></tr><tr><td>WI_</td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES	HIGH CONTRAST	WI_	Writes "I".
LS	RS	R/W																											
0	1	0																											
DB ₇	~				DB ₀																								
0	1	0	0	1	0	0	1																						
LCD MODULE DMC40																													
160 DIGITS, 4 LINES																													
HIGH CONTRAST																													
WI_																													

No.	Instruction	Display	Operation																							
25																										
26	<table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>0</td><td>1</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td></td><td>~</td><td></td><td>DB₀</td></tr><tr><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td></tr></table>	LS	RS	R/W	0	1	0	DB ₇		~		DB ₀	0	1	0	0	0	1	0	1	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES</td></tr><tr><td>HIGH CONTRAST</td></tr><tr><td>WIDE VIEWING ANGLE</td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES	HIGH CONTRAST	WIDE VIEWING ANGLE	Writes "E".
LS	RS	R/W																								
0	1	0																								
DB ₇		~		DB ₀																						
0	1	0	0	0	1	0	1																			
LCD MODULE DMC40																										
160 DIGITS, 4 LINES																										
HIGH CONTRAST																										
WIDE VIEWING ANGLE																										
27	Display ON/OFF control <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>0</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td></td><td>~</td><td></td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr></table>	LS	RS	R/W	0	0	0	DB ₇		~		DB ₀	0	0	0	0	1	1	0	0	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES</td></tr><tr><td>HIGH CONTRAST</td></tr><tr><td>WIDE VIEWING ANGLES</td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES	HIGH CONTRAST	WIDE VIEWING ANGLES	Turns the cursor off.
LS	RS	R/W																								
0	0	0																								
DB ₇		~		DB ₀																						
0	0	0	0	1	1	0	0																			
LCD MODULE DMC40																										
160 DIGITS, 4 LINES																										
HIGH CONTRAST																										
WIDE VIEWING ANGLES																										
28	Set DD RAM address <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>1</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td></td><td>~</td><td></td><td>DB₀</td></tr><tr><td>1</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr></table>	LS	RS	R/W	1	0	0	DB ₇		~		DB ₀	1	0	0	0	0	0	0	0	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES</td></tr><tr><td>HIGH CONTRAST</td></tr><tr><td>WIDE VIEWING ANGLE</td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES	HIGH CONTRAST	WIDE VIEWING ANGLE	Sets DD RAM address to the 1st line.
LS	RS	R/W																								
1	0	0																								
DB ₇		~		DB ₀																						
1	0	0	0	0	0	0	0																			
LCD MODULE DMC40																										
160 DIGITS, 4 LINES																										
HIGH CONTRAST																										
WIDE VIEWING ANGLE																										
29	Display ON/OFF control <table><tr><td>LS</td><td>RS</td><td>R/W</td></tr><tr><td>1</td><td>0</td><td>0</td></tr></table> <table><tr><td>DB₇</td><td></td><td>~</td><td></td><td>DB₀</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr></table>	LS	RS	R/W	1	0	0	DB ₇		~		DB ₀	0	0	0	0	1	1	1	0	<table><tr><td>LCD MODULE DMC40</td></tr><tr><td>160 DIGITS, 4 LINES</td></tr><tr><td>HIGH CONTRAST</td></tr><tr><td>WIDE VIEWING ANGLE</td></tr></table>	LCD MODULE DMC40	160 DIGITS, 4 LINES	HIGH CONTRAST	WIDE VIEWING ANGLE	Turn the cursor on at the 1st digit of the 1st line.
LS	RS	R/W																								
1	0	0																								
DB ₇		~		DB ₀																						
0	0	0	0	1	1	1	0																			
LCD MODULE DMC40																										
160 DIGITS, 4 LINES																										
HIGH CONTRAST																										
WIDE VIEWING ANGLE																										
30																										

(4) In case interface data length is 4-bit (DMC 16207)

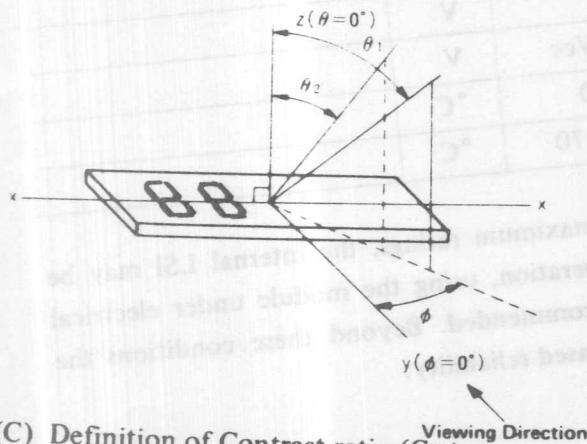
No.	Instruction	Display	Operation																			
1	Power supply on (initialized by internal circuit) <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₄</td></tr><tr><td></td><td></td><td></td><td></td><td></td></tr></table>	RS	R/W	DB ₇	~	DB ₄						<table><tr><td></td></tr><tr><td></td></tr></table>			Module is initialized.							
RS	R/W	DB ₇	~	DB ₄																		
2	Function set <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₄</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr></table>	RS	R/W	DB ₇	~	DB ₄	0	0	0	0	1	0	<table><tr><td></td></tr><tr><td></td></tr></table>			Set the interface data length to 4 bits. Since module has been 8 bits by initial set, instruction is required only one time.						
RS	R/W	DB ₇	~	DB ₄																		
0	0	0	0	1	0																	
3	Function set <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₄</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>X</td><td>X</td><td>X</td></tr></table>	RS	R/W	DB ₇	~	DB ₄	0	0	0	0	1	0	0	0	1	X	X	X	<table><tr><td></td></tr><tr><td></td></tr></table>			Set the interface data length to 4 bits and select 2-line display and 5 x 7-dot character font. Since it is operated as 4 bits from here, re-set is necessary.
RS	R/W	DB ₇	~	DB ₄																		
0	0	0	0	1	0																	
0	0	1	X	X	X																	
4	Display ON/OFF control <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₄</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td></tr></table>	RS	R/W	DB ₇	~	DB ₄	0	0	0	0	0	0	0	0	1	1	1	0	<table><tr><td>—</td></tr><tr><td></td></tr></table>	—		Turn on display and cursor. No display appear.
RS	R/W	DB ₇	~	DB ₄																		
0	0	0	0	0	0																	
0	0	1	1	1	0																	
—																						
5	Entry mode set <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₄</td></tr><tr><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td></tr></table>	RS	R/W	DB ₇	~	DB ₄	0	0	0	0	0	0	0	0	0	1	1	0	<table><tr><td>—</td></tr><tr><td></td></tr></table>	—		Set mode to increment address by one and shift the cursor to the right at the time of write to internal RAM.
RS	R/W	DB ₇	~	DB ₄																		
0	0	0	0	0	0																	
0	0	0	1	1	0																	
—																						
6	Write data to CG/DD RAM <table><tr><td>RS</td><td>R/W</td><td>DB₇</td><td>~</td><td>DB₄</td></tr><tr><td>1</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td></tr></table>	RS	R/W	DB ₇	~	DB ₄	1	1	0	1	0	0	1	0	1	1	0	0	<table><tr><td>L</td></tr><tr><td></td></tr></table>	L		Write "L". Cursor is incremented by one and shift to the right.
RS	R/W	DB ₇	~	DB ₄																		
1	1	0	1	0	0																	
1	0	1	1	0	0																	
L																						

3. OPTICAL CHARACTERISTICS

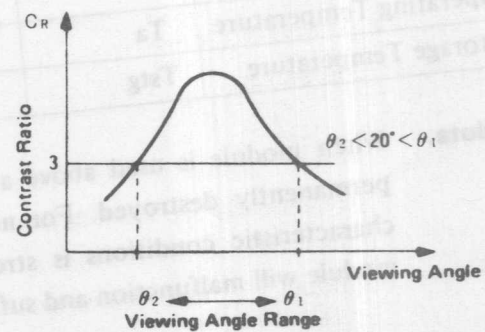
Item	Symbol	Condition	Specs. value			Unit
			Min.	Typ.	Max.	
LC Drive Voltage (Recommended value) 1/8 duty	$V_{cc} \sim V_{ee}$ (VD)	$T_a = 0^\circ\text{C}$	4.0	—	—	V
		$T_a = 25^\circ\text{C}$	—	4.1	—	V
		$T_a = 50^\circ\text{C}$	—	—	4.2	V
Range of viewing angle	$\theta_1 - \theta_2$	CR = 3	30	—	—	deg.
Contrast ratio	CR	$\theta_2 = 20^\circ, \phi = 0^\circ$	10	—	—	—
Rising time	τ_r	$V_D = 4.1\text{V}, \theta = 20^\circ$	—	100	200	ms
Decay time	τ_d	$V_D = 4.1\text{V}, \theta = 20^\circ$	—	100	200	ms
LC Drive Voltage (Recommended value) 1/11 duty	$V_{cc} \sim V_{ee}$ (VD)	$T_a = 0^\circ\text{C}$	4.4	—	—	V
		$T_a = 25^\circ\text{C}$	—	4.5	—	V
		$T_a = 50^\circ\text{C}$	—	—	4.6	V
Range of viewing angle	$\theta_1 - \theta_2$	CR = 3	25	—	—	deg.
Contrast ratio	CR	$\theta_2 = 20^\circ, \phi = 0^\circ$	8	—	—	—
Rising time	τ_r	$V_D = 4.5\text{V}, \theta = 20^\circ$	—	120	240	ms
Decay time	τ_d	$V_D = 4.5\text{V}, \theta = 20^\circ$	—	120	240	ms
LC drive voltage (Recommended value) 1/16 duty	$V_{cc} \sim V_{ee}$ (VD)	$T_a = 0^\circ\text{C}$	4.7	4.8	4.9	V
		$T_a = 25^\circ\text{C}$	4.4	4.5	4.6	V
		$T_a = 50^\circ\text{C}$	4.1	4.2	4.3	V
Range of viewing angle	$\theta_1 - \theta_2$	CR = 3	20	—	—	deg.
Contrast ratio	CR	$\theta_2 = 20^\circ, \phi = 0^\circ$	6	—	—	—
Rising time	τ_r	$V_D = 4.5\text{V}, \theta = 20^\circ$	—	120	240	ms
Decay time	τ_d	$V_D = 4.5\text{V}, \theta = 20^\circ$	—	120	240	ms

* $V_{cc} = 5.0\text{V} \pm 5\%$, $T_a = 25^\circ\text{C}$

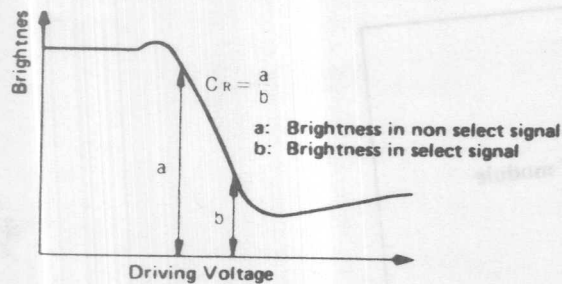
(A) Angle θ and definition of ϕ



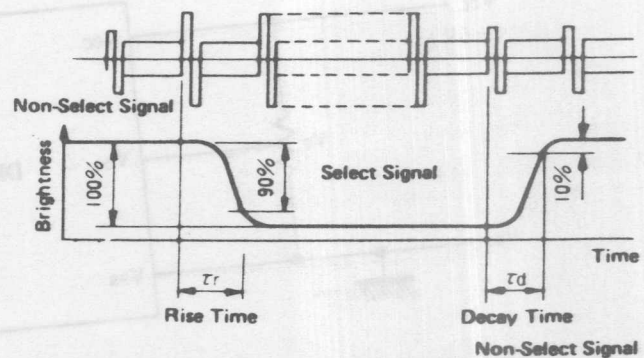
(B) Definition of viewing angles θ_2 and θ_1



(C) Definition of Contrast ratio (CR)



(D) Definition of optical response time



* τ_r is the time needed for the brightness of ON segment to reach from 0 to 90% and τ_d is the time needed for the same to decay from 100% to 10%.

4 ELECTRICAL CHARACTERISTICS

4.1 Absolute maximum ratings

MODULES EXCEPT FOR DMC 16433, DMC 20434

$V_{CC} = 5.0V \pm 5\%$, $T_a = 25^\circ C$

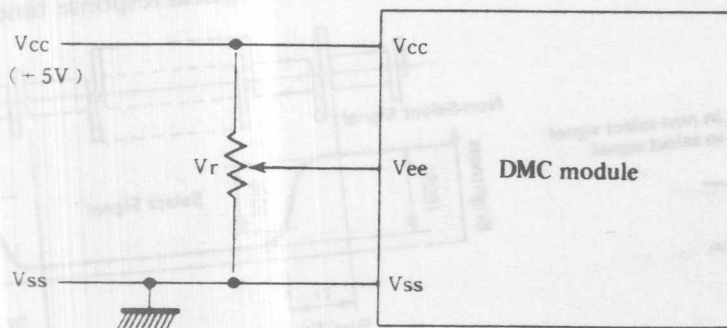
Item	Symbol	Specs. Value	Unit	Remarks
Supply voltage	$V_{CC} \sim V_{SS}$	$0 \sim 7.0$	V	
	$V_{CC} \sim V_{EE}$	$0 \sim 13.5$	V	
Input voltage	V_i	$V_{SS} \sim V_{CC}$	V	
Operating Temperature	T_a	$0 \sim +50$	$^\circ C$	
Storage Temperature	T_{stg}	$-20 \sim +70$	$^\circ C$	

DMC 16433, DMC 20434

$V_{CC} = 5.0V \pm 5\%$, $T_a = 25^\circ C$

Item	Symbol	Specs. Value	Unit	Remarks
Supply Voltage	$V_{CC} \sim V_{SS}$	$0 \sim 6.5$	V	
	$V_{CC} \sim V_{EE}$	$0 \sim 6$	V	
Input Voltage	V_i	$V_{SS} \sim V_{CC}$	V	
Operating Temperature	T_a	$0 \sim +50$	$^\circ C$	
Storage Temperature	T_{stg}	$-20 \sim +70$	$^\circ C$	

Note: When module is used above absolute maximum ratings, the internal LSI may be permanently destroyed. For normal operation, using the module under electrical characteristic conditions is strongly recommended. Beyond these conditions the module will malfunction and suffer decreased reliability.



4.2 Electrical characteristics ($V_{CC} = 5V \pm 5\%$, $T_a = 25^\circ C$)

Item	Symbol	Conditions	Specs. Value			Unit
			Min	Typ.	Max.	
Input Voltage	High	$V_{IH} 1$	2.2	—	V_{CC}	V
	Low	$V_{IL} 1$	-0.3	—	0.6	V
Output Voltage (TTL)	High	$V_{OH} 1$ $-I_{OH} = 0.205mA$	2.4	—	—	V
	Low	$V_{OL} 1$ $I_{OL} = 1.2mA$	—	—	0.4	V
Output Voltage (CMOS)	High	$V_{OH} 2$ $-I_{OH} = 0.04mA$	$0.9 V_{CC}$	—	—	V
	Low	$V_{OL} 2$ $I_{OL} = 0.04mA$	—	—	$0.1 V_{CC}$	V

Note: E signal terminal is not pulled up. Be sure to make it "H" or "L" when using the module.

4.3 Timing characteristics

(1) Write operation

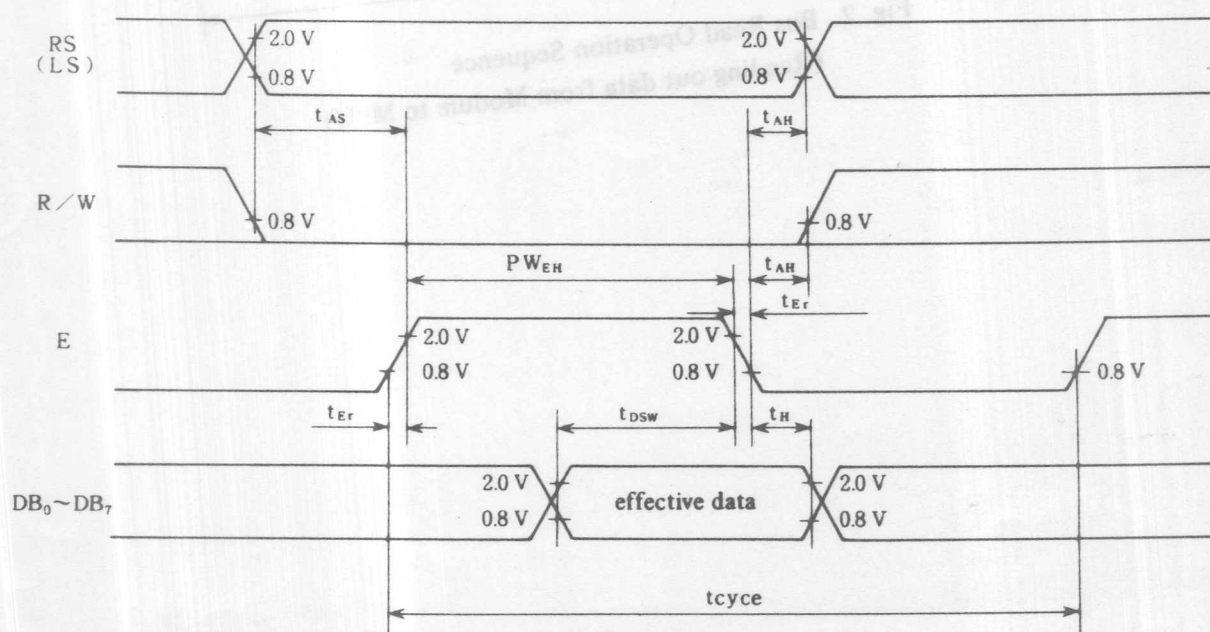


Fig. 1 Bus write operation Sequence.
(Writing data from MPU to Module)

(2) Read operation

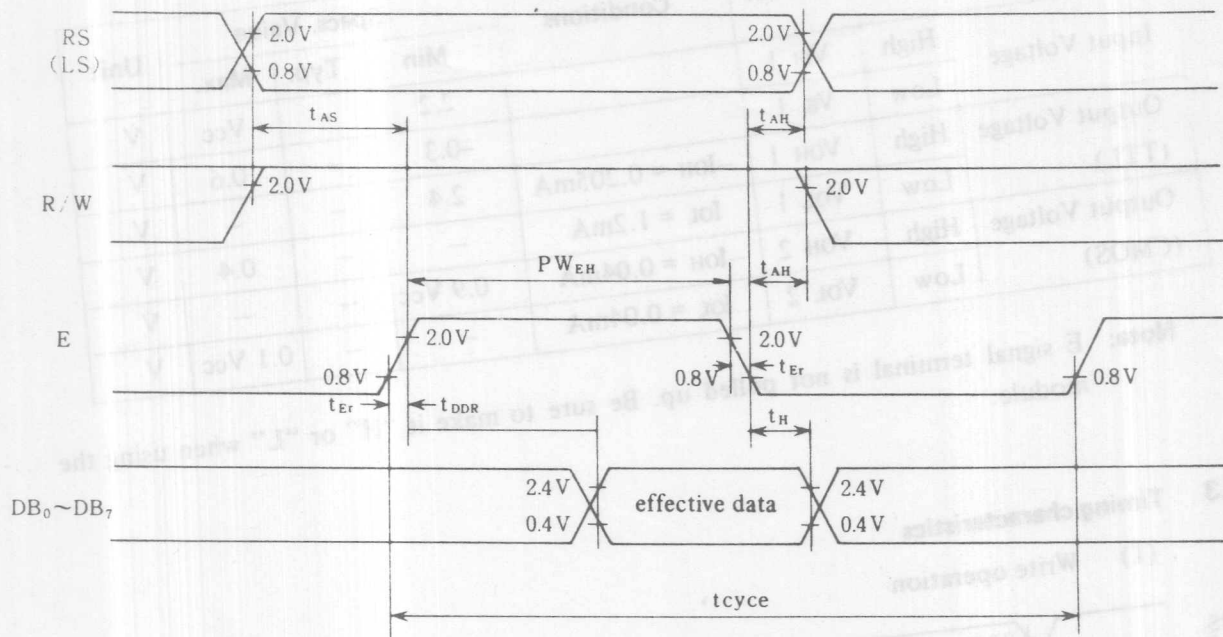


Fig. 2 Bus Read Operation Sequence
(Reading out data from Module to MPU)

- (3) Timing characteristics of each drawing ($V_{cc} = 5.0V \pm 5\%$, $V_{ss} = 0V$,
 $T_a = 0 \sim 50^\circ C$)

(a) Write timing characteristics (Fig. 1)

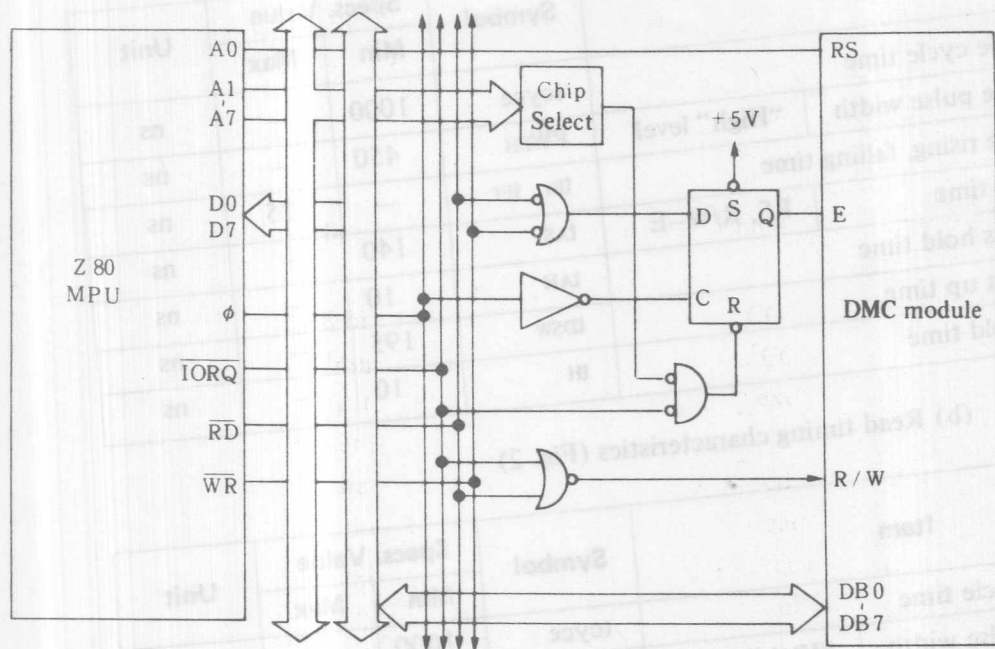
Item		Symbol	Specs. Value		Unit
			Min	Max	
Enable cycle time		t _{cyce}	1000	—	ns
Enable pulse width	“High” level	P _{WEH}	450	—	ns
Enable rising, falling time		t _{Er} , t _{Ef}	—	25	ns
Set up time	RS, R/W—E	t _{AS}	140	—	ns
Address hold time		t _{AH}	10	—	ns
Data set up time		t _{DSW}	195	—	ns
Data hold time		t _H	10	—	ns

(b) Read timing characteristics (Fig. 2)

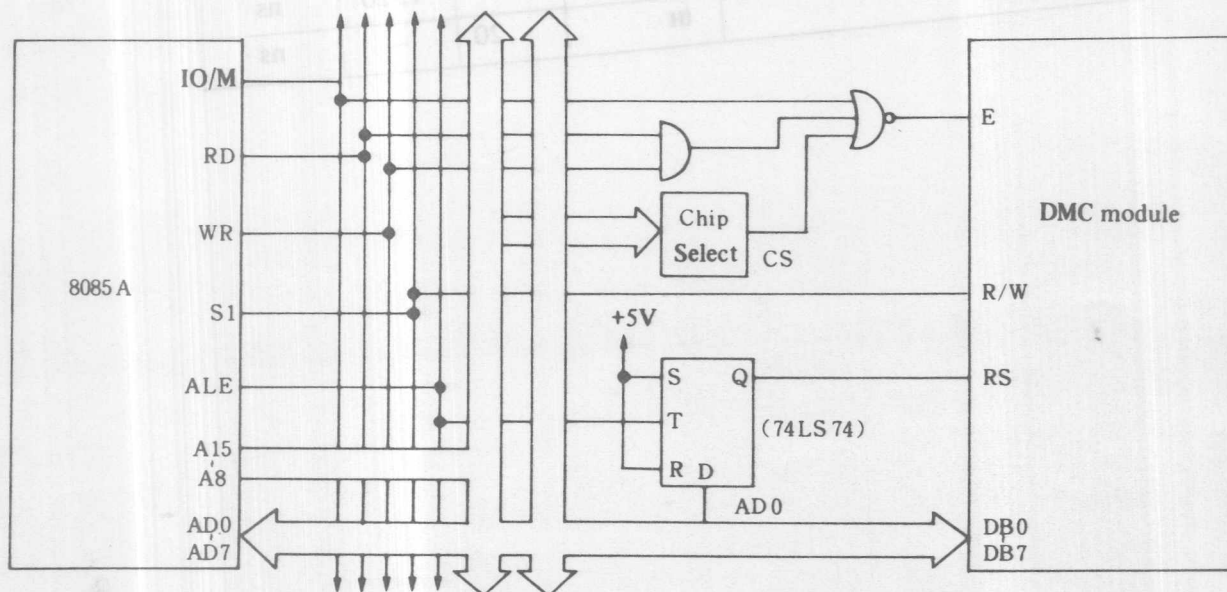
Item		Symbol	Specs. Value		Unit
			Min	Max	
Enable cycle time		t _{cyce}	1000	—	ns
Enable pulse width	“High” level	P _{WEH}	450	—	ns
Enable rise, fall time		t _{Er} , t _{Ef}	—	25	ns
Set up time	RS, R/W—E	t _{AS}	140	—	ns
Data delay time		t _{DDR}	—	1320	ns
Data hold time		t _H	20	—	ns

5. CONNECTION DIAGRAM WITH MPU

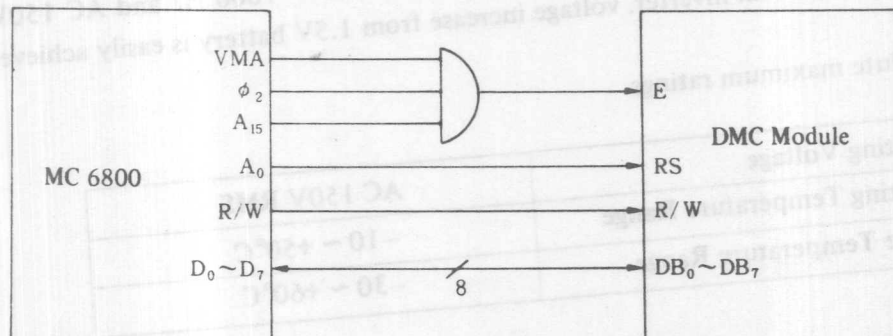
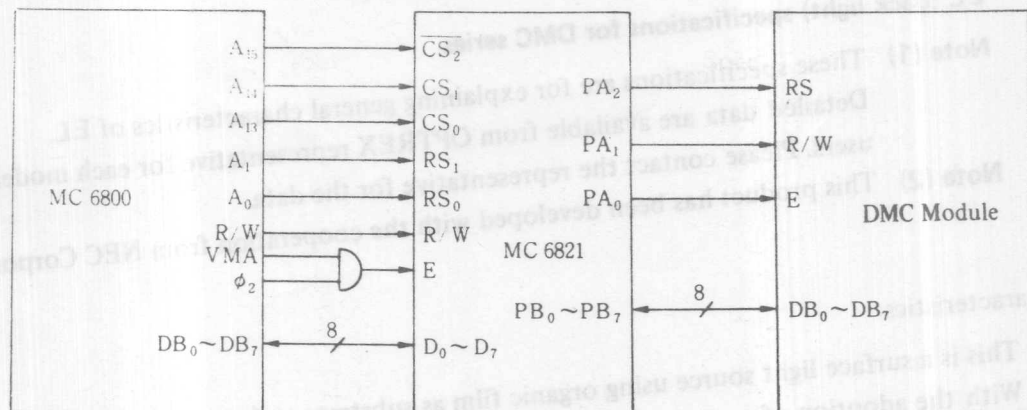
5.1 Connection with Z-80



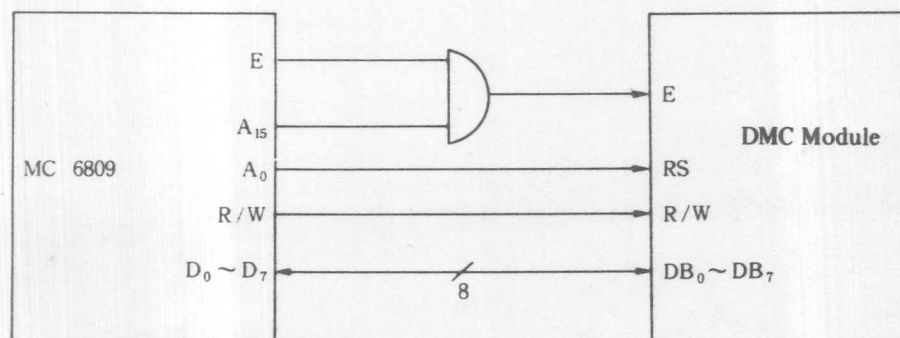
5.2 Connection with 8085A



5.3 Connection with MC 6800



5.4 Connection with MC 6809



6. SPECIAL SPECIFICATIONS

6.1 EL (back light) specifications for DMC series

Note (1) These specifications are for explaining general characteristics of EL.

Detailed data are available from OPTREX representative for each model to assist users. Please contact the representative for the data.

Note (2) This product has been developed with the cooperation from NEC Corporation.

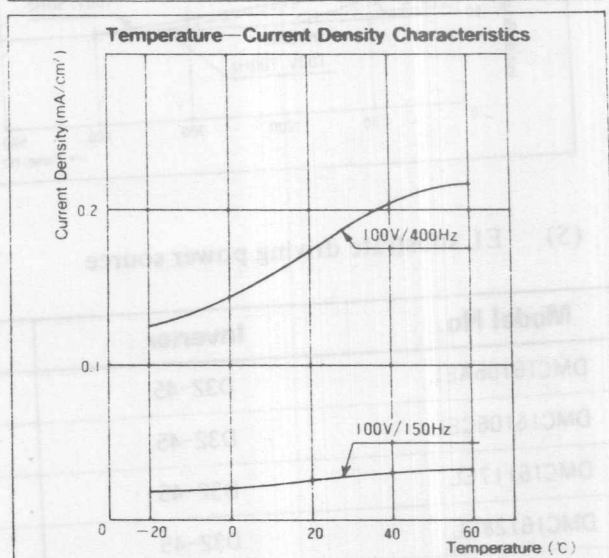
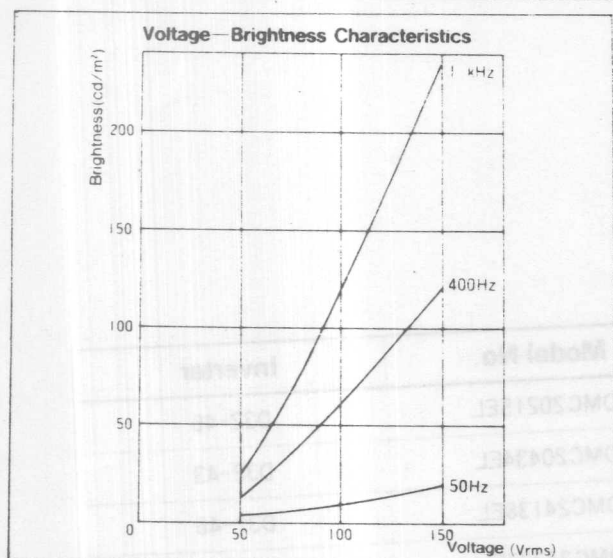
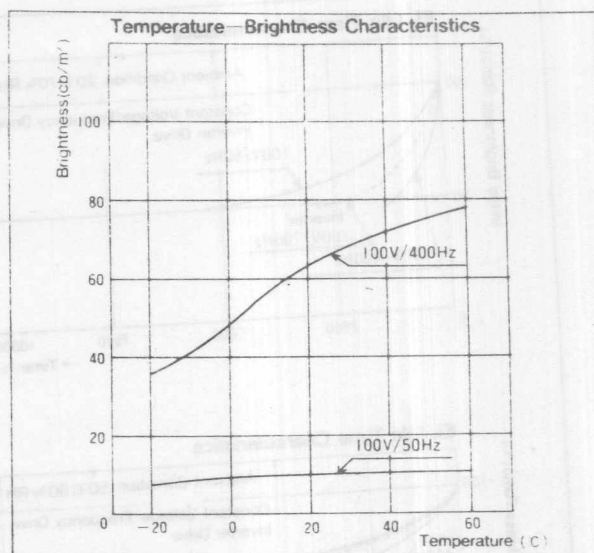
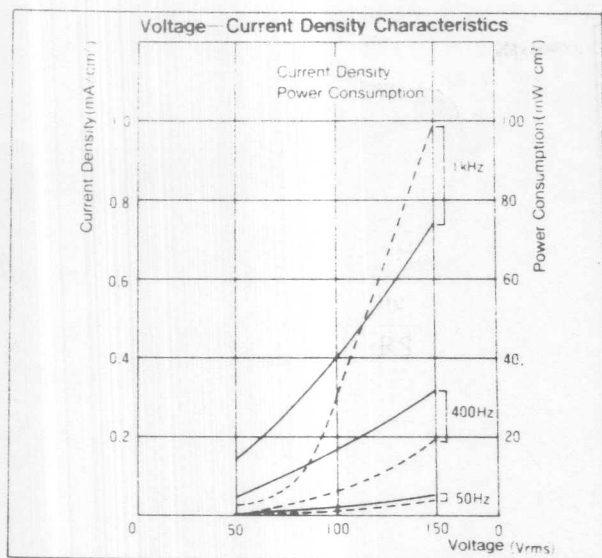
◆ Characteristics

- This is a surface light source using organic film as substrate and packaging material.
- With the adoption of new materials and production process, the thickness is reduced to 1.3 mm Max. (Electrode portion is 1.5 mm Max.) making it suited for high density mount.
- Color emission is blue green.
- Driving voltage can be selected from a wide range of 60 ~ 1000 Hz and AC 150V Max. Also with the help of an inverter, voltage increase from 1.5V battery is easily achieved.

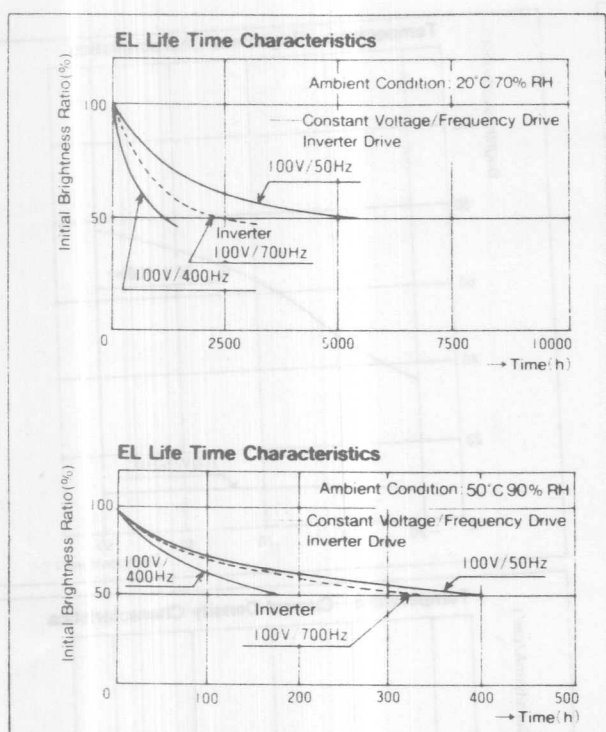
(1) Absolute maximum ratings

Operating Voltage	AC 150V RMS
Operating Temperature Range	-10 ~ +50°C
Storage Temperature Range	-30 ~ +60°C

(2) Electrical characteristics (Color emission: Blue green)



(3) Life characteristics



(5) EL substrate driving power source

Model No.	Inverter	Model No.	Inverter
DMC16106AEL	D32-45	DMC20215EL	D32-46
DMC16106CEL	D32-45	DMC20434EL	D32-43
DMC16117EL	D32-45	DMC24138EL	D32-46
DMC16128EL	D32-45	DMC24227EL	D32-46
DMC16129EL	D32-45	DMC32132EL	D32-43
DMC16106BEL	D32-45	DMC32216EL	D32-43
DMC16207EL	D32-45	DMC40131EL	D32-43
DMC16230EL	D32-43	DMC40218EL	D32-43
DMC16433EL	D32-43		

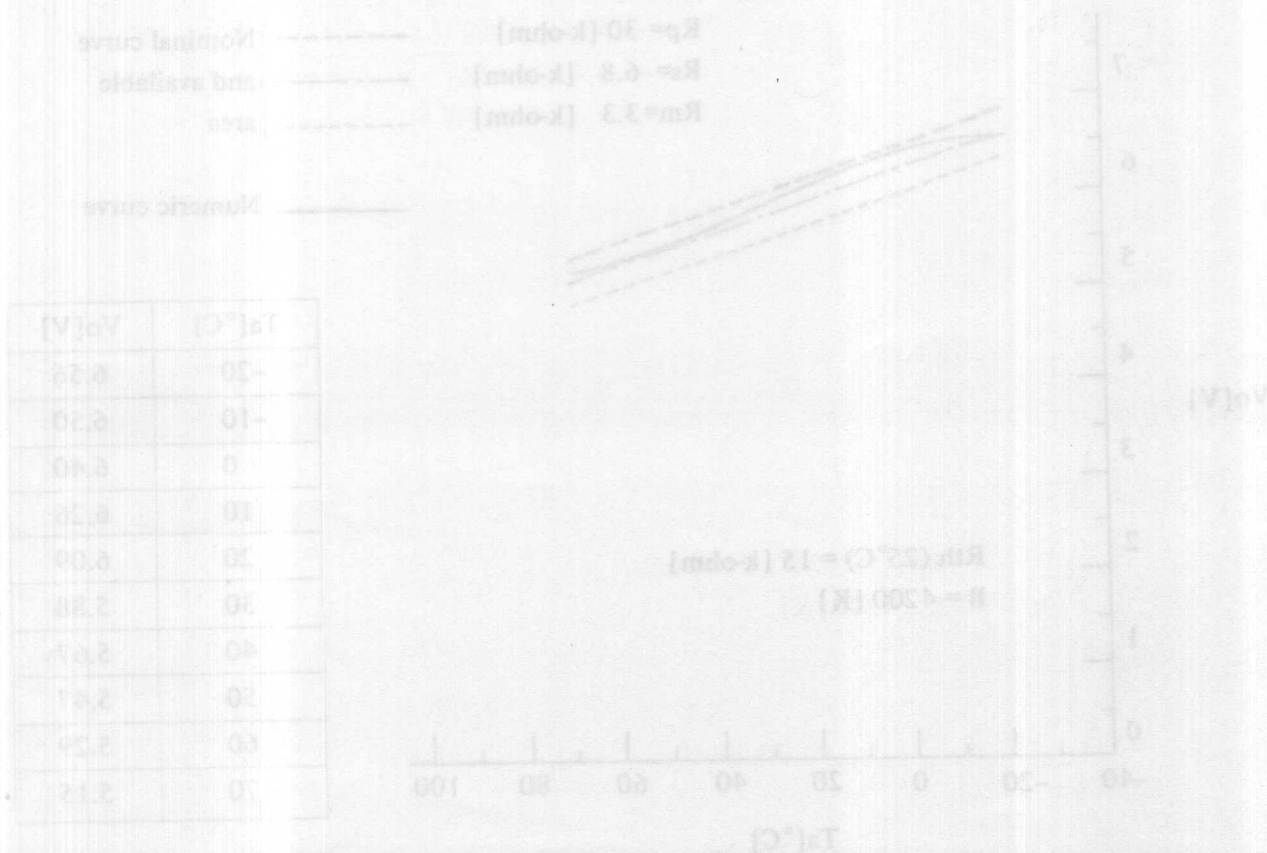
6.2 High reliability specifications

Among the DMC series, some of the modules are made to meet high reliability specs., using liquid crystal usable within a wide range of temperature. Those modules have an "H" in their type names to distinguish from the others.

However, as modules of high reliability use liquid crystal and power source of different characteristics caution is invited when putting them to use.

- (1) Operating Temperature $-20^{\circ}\text{C} \sim +70^{\circ}\text{C}$
- (2) Storage Temperature $-30^{\circ}\text{C} \sim +80^{\circ}\text{C}$

Note: Even in these "H" modules, the specifications for EL Backlight are standard level (p. 42 ~ 44).



6.3 Examples of Temperature Compensation circuits (Only for reference)

(A) 1/8 Duty – 1/3 Bias

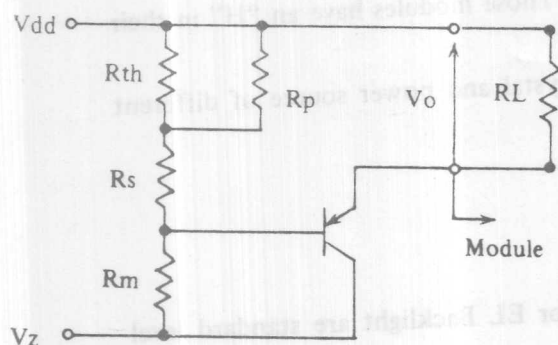


Fig. 1

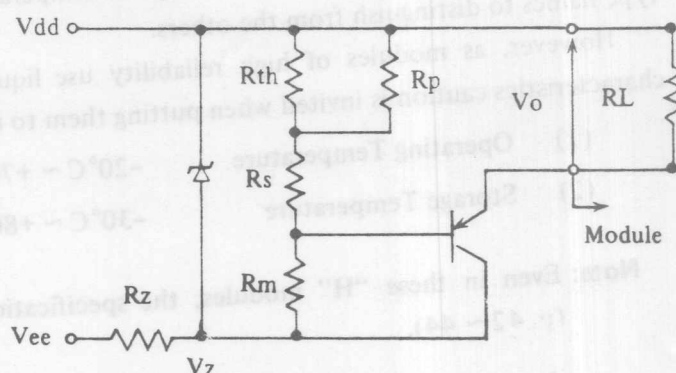


Fig. 2

Thermistor : $R_{th}(25^{\circ}\text{C}) = 15[\text{k-ohm}]$, $B = 4200[\text{K}]$

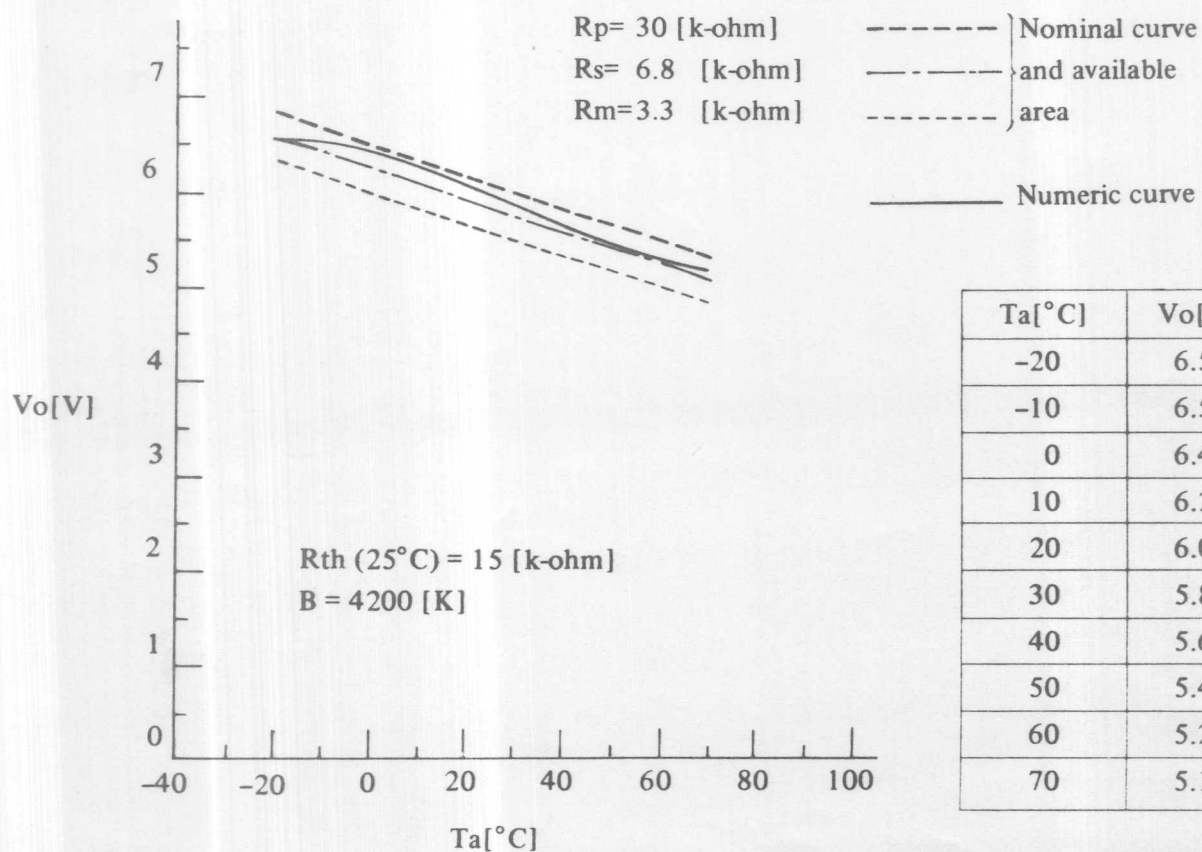
Resistors : $R_p = 30[\text{k-ohm}]$, $R_s = 6.8[\text{k-ohm}]$, $R_m = 3.3[\text{k-ohm}]$

Transistor : PNP Type

$V_{dd} : 0[\text{V}]$, $V_{ss} : -5[\text{V}]$ (Logic Supply)

$V_z : -8[\text{V}]$ (-7.8 to $-8.2[\text{V}]$)

$V_{ee} < V_z [\text{V}]$, $R_z = (V_z - V_{ee})/5 [\text{k-ohm}]$



* Specifications are subject to change without notice.

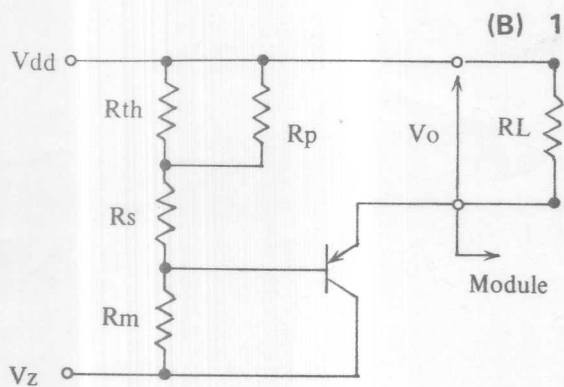


Fig. 1

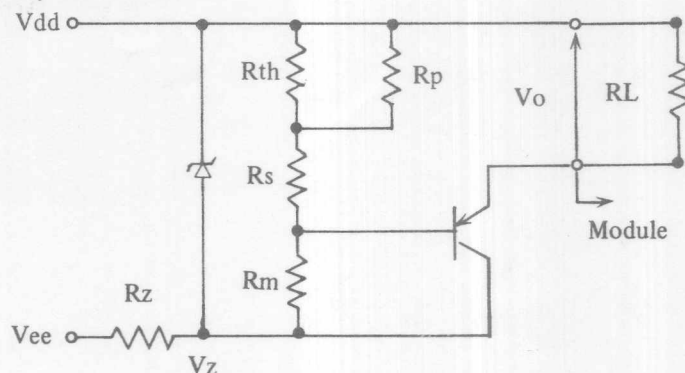
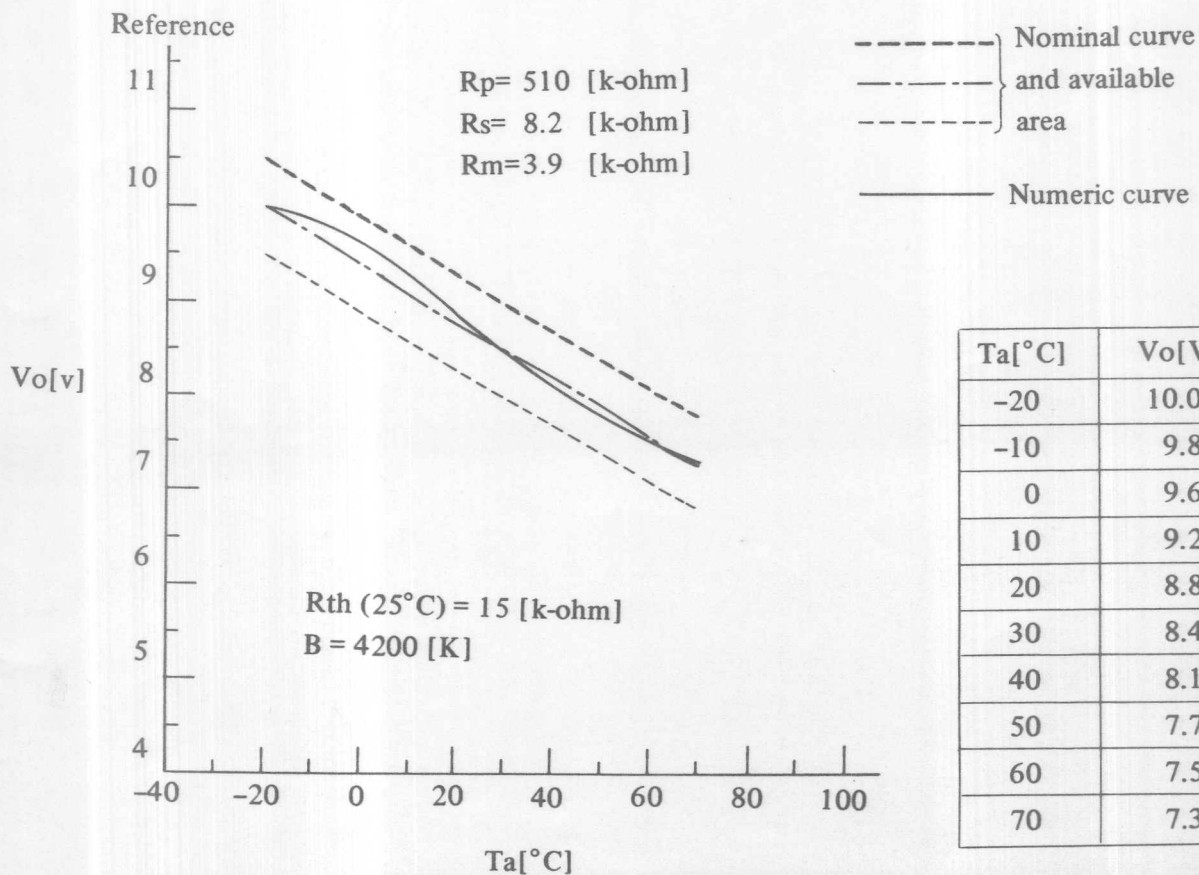


Fig. 2

Thermistor : $R_{th}(25^{\circ}\text{C}) = 15[\text{k-ohm}]$, $B = 4200[\text{K}]$
 Resistors : $R_p = 510[\text{k-ohm}]$, $R_s = 8.2[\text{k-ohm}]$, $R_m = 3.9[\text{k-ohm}]$
 Transistor : PNP Type
 $V_{dd} : 0[\text{V}]$, $V_{ss} : -5[\text{V}]$ (Logic Suply)
 $V_z : -11[\text{V}]$ (-10.725 to $-11.275[\text{V}]$)
 $V_{ee} < V_z [\text{V}]$, $R_z = (V_z - V_{ee})/5 [\text{k-ohm}]$



* Specifications are subject to change without notice.

